1Mb Quad SPI nvSRAM

FEATURES

- **Compatible with Serial Peripheral Interface (SPI)**
- **Supports SPI Modes 0 and 3**
- **Interface options with Single SPI, Dual SPI and Quad SPI**
- **Interface options separately controlled for Instruction, Address and Data**
- **Modes: Standard, Burst and XIP**
- **108 MHz clock rate**
- **Block Write Protection**
- **Write Disable Instruction for Software Data Protection**
- **WRITE and Secure WRITE**
- **READ, fast READ and Secure READ**
- **16 Byte User Serial Number**
- **Configuration and Status Register**
- **Low Power Hibernate (HIB <3µA) Mode**
- **Unlimited READ / WRITE Endurance**
- **Automatic Non-volatile STORE on Power Down**
- **Non-Volatile STORE under Instruction and $\overline{\text{HSB}}$ Control**
- **Automatic RECALL to SRAM on Power-Up**
- **Unlimited RECALL Cycles**
- **100k STORE Cycles**
- **100-Year Non-volatile Data Retention**
- **2.7V to 3.6V main Power Supply**
- **1.65V to 1.95V I/O Power Supply**
- **Commercial and Industrial Temperatures**
- **24 Ball BGA Package (6 x 8)**
- **RoHS-Compliant**

DESCRIPTION

The Anvo-Systems Dresden ANV32AA3P is a 1Mb Quad SPI SRAM with a non-volatile SONOS storage element included with each memory cell, organized as 128k words of 8 bits each. The devices are accessed by a high speed Quad SPI-compatible bus. There are different SPI options available: SPI, DPI and QPI. Additionally, in single SPI mode the address bytes and/or the data byte(s) can be clocked in using dual or quad interface. The ANV32AA3P is enabled through the Chip Enable pin ($\overline{\text{E}}$), accessed via serial clock (CLK) and 3 operation modes either with single serial data input (SI) and single serial data output (SO) or dual by 2 bidirectional input / outputs (I/O0 and I/O1) or quad by 4 bidirectional inputs / outputs (I/O0, I/O1, I/O2, I/O3).

The Quad SRAM interface provides the fast access & cycle times, ease of use and unlimited READ & WRITE endurance of a standard SRAM. Dedicated safety features support high data accuracy.

With Secure WRITE operation the ANV32AA3P accepts address and data only when the correct 2 Byte CRC, generated from the complete 3 address Bytes and 128 Byte data, has been transmitted. Corrupt data cannot overwrite existing memory content and even valid data would not overwrite on a corrupted address. With configuration register bit 4 the success of the Secure WRITE operation can be monitored. In case of corrupt data, bit 4 will be set volatile to high.

With Secure READ operation the ANV32AA3P calculates the correct 2 Byte CRC parallel to data transfer. The 2 Byte CRC is transmitted after 128 Bytes of data have been read out.

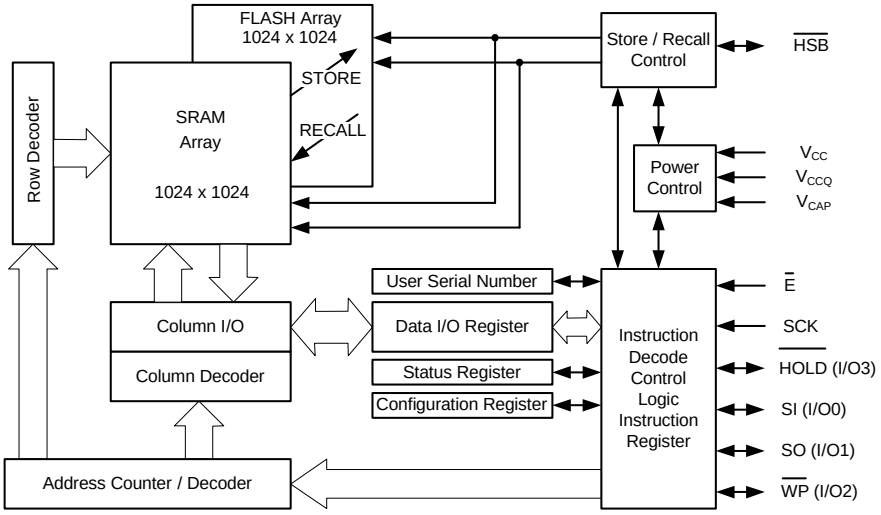
Data transfer automatically to the non-volatile storage cells when power loss is detected or in any brown out situation (the PowerSTORE operation). On power-up, data are automatically restored to the SRAM (the Power-Up RECALL operation). The PowerSTORE operation can be disabled via Configuration Register settings.

Both STORE and RECALL operations are also available under instruction control, STORE can also be hardware controlled via $\overline{\text{HSB}}$ pin.

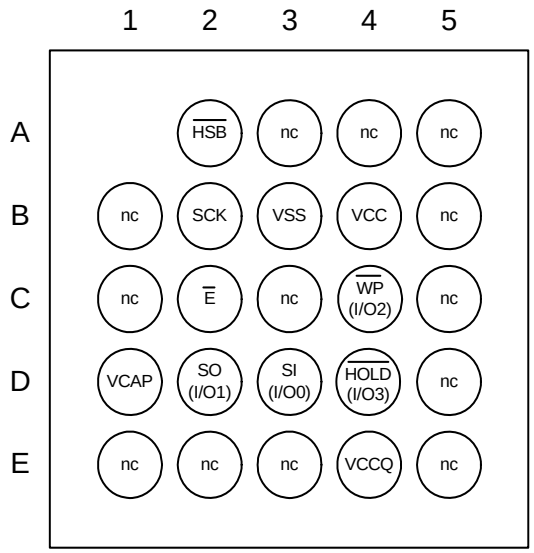
BLOCK WRITE Protection is enabled by programming the status register with 1 of 14 options to protect blocks of the memory.

A non-volatile register supports the option of a 8 Byte user defined serial number. This register is under customer control only.

BLOCK DIAGRAM



PIN CONFIGURATION



BGA24 Top View

PIN DESCRIPTIONS

Signal Name	Signal Description
$\overline{E}$	Chip Enable
SCK	Serial Clock
SI or I/O0	Serial Input (SPI Mode) I/O [0] in dual or quad mode
SO or I/O1	Serial Output (SPI Mode) I/O [1] in dual or quad mode
$\overline{HOLD}$ or I/O3	Hold (Suspends Serial Input) I/O [3] in quad mode
$\overline{WP}$ or I/O2	Write Protect I/O [2] in quad mode
$\overline{HSB}$	Hardware Store busy
VCC	Main Power Supply Voltage
VCCQ	I/O Power Supply Voltage
VCAP	Capacitor Voltage
VSS	Ground

Serial Interface Description

Master: The device that generates the serial clock.

Slave: Because the Serial Clock pin (SCK) is always an input, the device always operates as a slave.

Transmitter/Receiver: The device has bi-directional pins (SI, I/O0, SO, I/O1, HOLD, I/O3, WP, I/O2 and HSB) designated for data transmission and reception. In SPI and DPI mode HOLD and WP act as inputs only.

Output: The SO, I/O0, I/O1, I/O2 and I/O3 pins are used in read cycles to transfer data out of the device after the falling edge of Serial Clock.

Input: The SI, I/O0, I/O1, I/O2 and I/O3 pins are used to transfer data into the device. They receive instructions, addresses, and data. Data are latched on the rising edge of the Serial Clock.

Serial Clock: The SCK pin is used to synchronize the communication between a master and the device. Instructions, addresses, or data, present on the input pin, are latched on the rising edge of the clock, while data on the output pins are changed after the falling edge of the clock input.

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

Serial Op-Code: After the device is selected with $\overline{E}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

Invalid Op-Code: If an invalid op-code is received, no data will be shifted into the device, and the output pins will remain in a high impedance state until the falling edge of $\overline{E}$ is detected. This will reinitialize the serial communication.

Chip Enable: The device is selected when the $\overline{E}$ pin is low. When the device is not selected ($\overline{E}$ pin is high), data will not be accepted via the input pins, and the output pins will remain in a high impedance state. Unless an internal WRITE cycle is in progress the device will be in the Standby Mode. Driving Chip Enable ($\overline{E}$) Low enables the device, placing it in the active power mode. After power-up a falling edge on Chip Enable ($\overline{E}$) is required prior to the start of any instruction.

Write Protect: The main purpose of this input signal is to freeze the size of the area of memory that is protected against WRITE instructions (as specified by the values in the BP2, BP1 and BP0 bits of the Status Register) and the selected PowerSTORE mode. This pin must be driven either High or Low, and must be stable during all WRITE operations.

Hold: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{E}$ pin to select the device. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence.

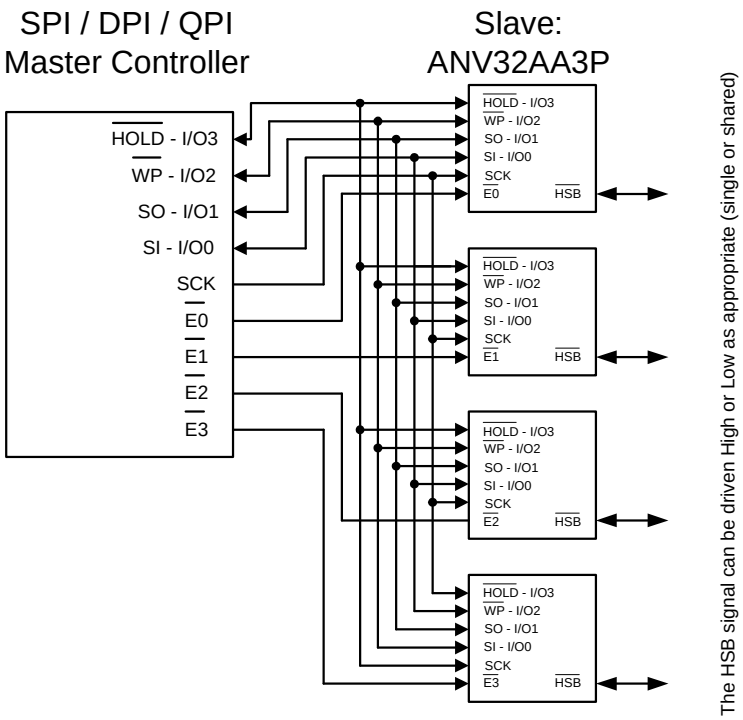
HSB: The $\overline{HSB}$ pin monitors a STORE operation in progress when driving the pin Low (output). A HardwareSTORE operation can be initiated by driving this pin low (input).

Buffer Cap: The VCAP pin provides the necessary energy for the PowerSTORE operation, via an external capacitor.

Connecting to the SPI Bus

These devices are fully compatible with the SPI protocol.
All instructions, addresses and input data bytes are shifted in to the device most significant bit first. The Serial Input (SI) is sampled on the first rising edge of the Serial Clock (SCK) after Chip Enable ($\overline{E}$) goes Low. All output data bytes are shifted out after any read instruction, most significant bit first. The Serial Output (SO) is latched on the first falling edge of the Serial Clock (SCK) after the instruction (such as the READ from Memory Array, Secure READ and READ Status Register instructions) has been clocked into the device.
The Figure shows four devices, connected to a MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (SO) line at a time, all the others being in high impedance.

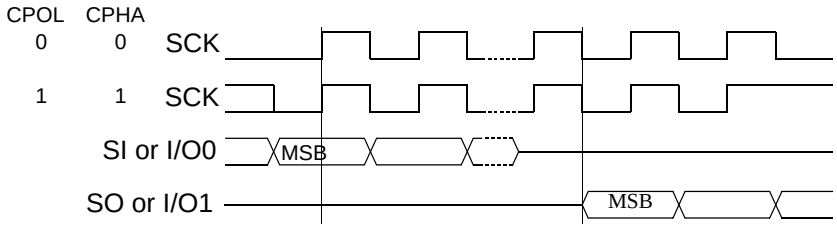
SPI BUS Connection



SPI Modes

Each device can be driven by a microcontroller with its SPI peripheral running in either of the following two modes:
- Mode 0: CPOL=0, CPHA=0
- Mode 3: CPOL=1, CPHA=1

For these two modes, input data have been latched with the rising edge of Serial Clock (SCK), and output data is available from the falling edge of Serial Clock (SCK). The difference between the two modes, as shown for single SPI access in the following figure, is the clock polarity when the bus master is in Stand-by mode and not transferring data:
- SCK remains at 0 for (CPOL=0, CPHA=0)
- SCK remains at 1 for (CPOL=1, CPHA=1)



Dual and Quad I/O Modes

Beside the standard SPI interface, a command controlled reconfiguration of SI, SO (Dual Mode with I/O0 and I/O1), or SI, SO, HOLD and WP (Quad Mode with I/O0, I/O1, I/O2 and I/O3) can be executed. In these modes all READ operations will require dummy cycles in contrast to WRITE operations which will require no ones. Parallelism can be enabled for op-code, address and data or for address and data or just for data. READ and WRITE operations can then be carried out in these parallel modes. Secure READ, Secure F_READ and Secure WRITE operations are available for SPI, DPI and QPI Modes. There is a detailed description under Functional Description later on.

Mode	Command	Command input	Address input	DMY/ MB cycles	Data input	Data output
SPI	READ	SI	SI	0		SO
SPI	S_READ	SI	SI	0		SO
SPI	F_READ	SI	SI	8		SO
SPI	FS_READ	SI	SI	8		SO
SPI	DOR	I/O0	I/O0	8		I/O0, I/O1
SPI	DIOR	I/O0	I/O0, I/O1	4		I/O0, I/O1
SPI	QOR	I/O0	I/O0	8		I/O0, I/O1, I/O2, I/O3
SPI	QIOR	I/O0	I/O0, I/O1, I/O2, I/O3	4		I/O0, I/O1, I/O2, I/O3
SPI	WRITE	SI	SI	0	SI	
SPI	S_WRITE	SI	SI	0	SI	
SPI	DIW	I/O0	I/O0	0	I/O0, I/O1	
SPI	DIOW	I/O0	I/O0, I/O1	0	I/O0, I/O1	
SPI	QIW	I/O0	I/O0	0	I/O0, I/O1, I/O2, I/O3	
SPI	QIOW	I/O0	I/O0, I/O1, I/O2, I/O3	0	I/O0, I/O1, I/O2, I/O3	
DPI	READ	I/O0, I/O1	I/O0, I/O1	1		I/O0, I/O1
DPI	S_READ	I/O0, I/O1	I/O0, I/O1	1		I/O0, I/O1
DPI	F_READ	I/O0, I/O1	I/O0, I/O1	4		I/O0, I/O1
DPI	FS_READ	I/O0, I/O1	I/O0, I/O1	4		I/O0, I/O1
DPI	WRITE	I/O0, I/O1	I/O0, I/O1	0	I/O0, I/O1	
DPI	S_WRITE	I/O0, I/O1	I/O0, I/O1	0	I/O0, I/O1	
QPI	READ	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1, I/O2, I/O3	1		I/O0, I/O1, I/O2, I/O3
QPI	S_READ	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1, I/O2, I/O3	1		I/O0, I/O1, I/O2, I/O3
QPI	F_READ	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1, I/O2, I/O3	2		I/O0, I/O1, I/O2, I/O3
QPI	FS_READ	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1, I/O2, I/O3	2		I/O0, I/O1, I/O2, I/O3
QPI	WRITE	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1, I/O2, I/O3	0	I/O0, I/O1, I/O2, I/O3	
QPI	S_WRITE	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1, I/O2, I/O3	0	I/O0, I/O1, I/O2, I/O3	

Operating Features

Power-up:
When the power supply is turned on from V_{SS}, Chip Enable ($\overline{E}$) has to follow the V_{CC} voltage in accordance with the definition of V_{IH}. It must not be allowed to float, but could be connected via a suitable pull-up resistor to V_{CC}. The Chip Enable signal ($\overline{E}$) is edge as well as level sensitive. This ensures that the device becomes deselected after Power-down until $\overline{E}$ reaches V_{CC} and a falling edge of $\overline{E}$ from the V_{IH} level has been detected thereafter. This will start the first operation.

Power-on Reset:
In order to prevent data corruption and inadvertent Write operations during power-up, all input signals will be ignored and Data Output will be in high impedance state. Power On Reset is completed when V_{CC} reaches a stable V_{CCmin}. Logical signals can be applied.

Power-down / Brown Out:
When V_{CC} drops during normal operation below V_{SWITCH} all external operations will be disabled, the device will ignore any input signals and Data Output will be in high impedance state. Power-down during self timed STORE operation will not corrupt data in the memory. WRITE operation of the current Byte will be completed independent from the power supply. Prior to any STORE operation the whole data in the non-volatile memory will be erased to allow STORE operation of new and restore of unchanged data.

Operating and Stand-by Modes:
When Chip Enable ($\overline{E}$) is Low, the device is enabled. In Operating Mode it is consuming $I_{CC(OP)}$. In the other case, when Chip Enable ($\overline{E}$) is High without prior Hibernate instruction, the device is in Standby Mode with the reduced Supply Current I_{SB}, with prior Hibernate instruction the Supply Current will be with I_{SBH} extreme low. To exit the Hibernate Mode Chip Enable ($\overline{E}$) has to go Low and after $t_{RESTORE}$ all operations can be executed.

Hold Condition:
The Hold ($\overline{HOLD}$) signal suspends any serial communication with the device without resetting the clock sequence.
Data Outputs are in high impedance state during Hold condition, $\overline{HOLD}$=Low. The other SPI-inputs are disabled and Don't Care.
The device has to be active with Chip Enable ($\overline{E}$) Low to enter the Hold condition. The device has to be selected for the duration of the Hold condition, for the selected operation to be continued after exiting the Hold condition. The Hold condition starts when Hold ($\overline{HOLD}$) becomes Low, the device is active with Chip Enable ($\overline{E}$) Low and Serial Clock (SCK) is already Low. The Hold conditions ends when Hold ($\overline{HOLD}$) goes High, the device is still active with Chip Enable ($\overline{E}$) Low and Serial Clock (SCK) is Low.
Chip Enable ($\overline{E}$) has priority over Hold ($\overline{HOLD}$). Driving Chip Enable ($\overline{E}$) High during Hold condition will reset the device. With the next falling edge of Chip Select ($\overline{E}$) a new instruction has to be submitted.

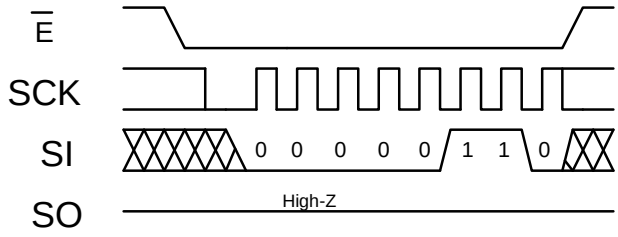
Functional Description

The device utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in the following table. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low $\overline{E}$ transition. Each instruction starts with one of the single-byte codes below. All instructions can be set and executed with clock up to 108 MHz, beside READ operations from the memory array (66 MHz).

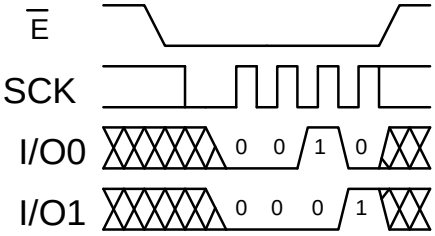
Instruction Name	Instruction format	Operation
WREN	0x06	Set Write Enable Latch
WRDI	0x04	Reset Write Enable Latch
SPIEN	0xFF	Enable SPI Mode (reset DPI, QPI)
DPIEN	0x37	Enable DPI Mode
QPIEN	0x38	Enable QPI mode
RDSR	0x05	Read Status Register
WRSR	0x01	Write Status Register
RDCR	0x35	Read Configuration Register
WRCR	0x87	Write Configuration Register
WRSNR	0xC2	WRITE User Serial Number
RDSNR	0xC3	READ User Serial Number
READ	0x03	Read Data from Memory Array
F_READ	0x0B	Fast Read Data from Memory Array
DOR	0x3B	Dual Output Read
DIOR	0xBB	Dual Input Output Read
QOR	0x6B	Quad Output Read
QIOR	0xEB	Quad Input output Read
S_READ	0x13	Secure Read Data from Memory Array with CRC
FS_READ	0x1B	Fast Secure Read Data Memory Array with CRC
WRITE	0x02	Write Data to Memory Array
DIW	0xA2	Dual Input Write
DIOW	0xA1	Dual Input Output Write
QIW	0x32	Quad Input Write
QIOW	0xD2	Quad Input Output Write
S_WRITE	0x12	Secure WRITE Data to Memory Array with CRC
Hibernate	0xB9	Enter Hibernate Mode
STORE	0x08	Store SRAM data non-volatile
RECALL	0x09	Recall non-volatile data to SRAM
	0xAF	Mode byte Start XIP
	0x0A	reserved
	0xBA	reserved
	0xFF	Mode byte Stop XIP

Write Enable (WREN):
The device will power up in the write disable state when V_{CC} is applied. Before any WRITE instruction is accepted, the Write Enable Latch has to be set with the WREN command.

As shown in the figure below, to send this instruction to the device, Chip Enable ($\overline{E}$) is driven Low, and the bits of the instruction byte are shifted in on Serial Data Input (SI). The device then enters a wait state, waiting for the device to be deselected, by Chip Enable ($\overline{E}$) being driven High.

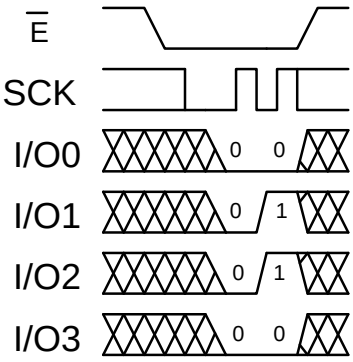


WREN SPI Mode



WREN DPI Mode

In DPI mode the instruction Byte will be shifted in on I/O0 (bit 6,4,2,0) and I/O1 (bit 7,5,3,1). In QPI mode analog via I/O0, I/O1, I/O2 and I/O3.

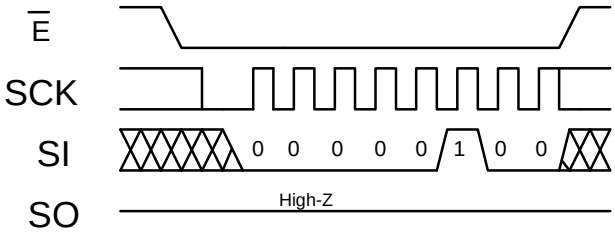


WREN QPI Mode

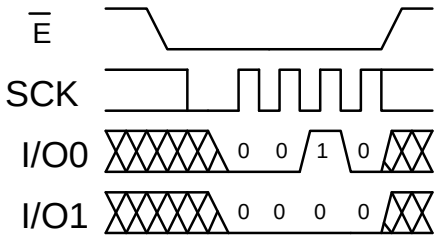
Write Disable (WRDI):
To protect the device against inadvertent writes, the Write Disable instruction disables all WRITE modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.
As shown in the figure below, to send this instruction to the device, Chip Enable ($\overline{E}$) is driven Low and the bits of the instruction byte are shifted in, on Serial Data Input (SI). The device then enters a wait state, waiting for the device to be deselected, by Chip Enable ($\overline{E}$) being driven High.

The Status Register Write Enable Latch (WEN) bit will be reset by any of the following events:

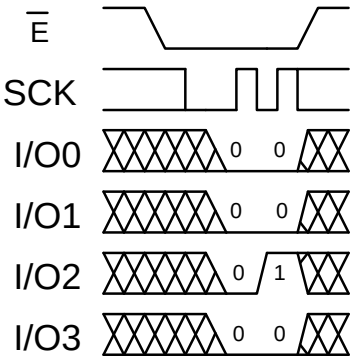
- Power-up
- WRDI, WRSR, WRCR, WRSNR instruction execution
- WRITE, S_WRITE instruction completion
- DIW, DIOW,QIW,QIOW instruction completion



WRDI SPI Mode



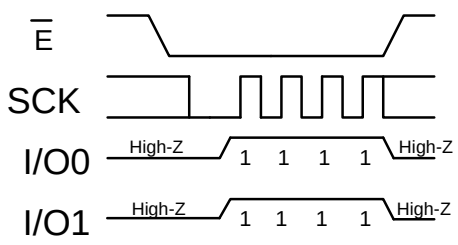
WRDI DPI Mode



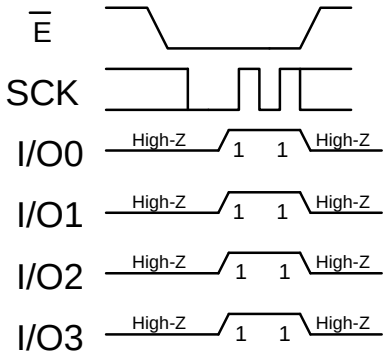
WRDI in QPI Mode

Enable SPI Mode (SPIEN)

With SPIEN instruction the 2 other Modes DPI and QPI can be volatile disabled. Configuration Register bit[1] will not be changed. SPIEN instruction has to be carried out in current DPI or QPI Mode.



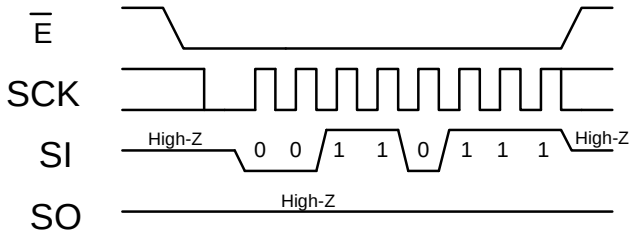
SPIEN in DPI Mode



SPIEN in QPI Mode

Enable DPI Mode

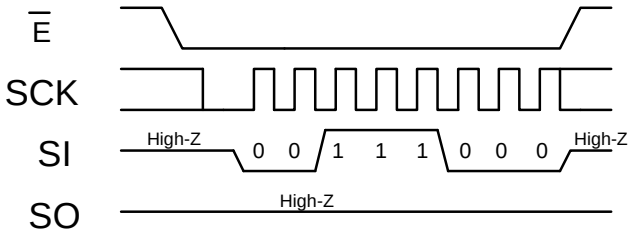
With DPIEN command SI [I/O0] and SO [I/O1] becomes bi-directional I/O pins. All communication for data, addresses, dummy bits, mode bits, instructions and register information will be executed in dual mode. DPIEN is a volatile setting. DPI Mode can only be activated out of SPI mode.



DPIEN in SPI Mode

Enable QPI Mode

With QPIEN instruction I/O0, I/O1, I/O2 and I/O3 become bidirectional I/O. All communication for data, addresses, dummy bits, mode bits, instructions and register information will be executed in quad mode. QPIEN is a volatile setting and overwrite temporarily the configuration register bit[1] until next power cycle. Configuration register stays unchanged. QPI Mode can only be activated out of SPI Mode.



QPIEN in SPI Mode

Status Register

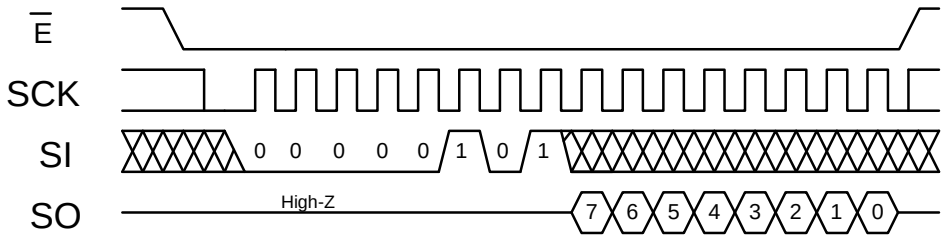
Status register is a 8 bit register with volatile and non-volatile bits which indicate the current capability to Write the ANV32AA3P (to indicate the Write protection status).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	PRSNR	SBP	BP3	BP1	BP0	WEN	$\overline{\text{RDY}}$

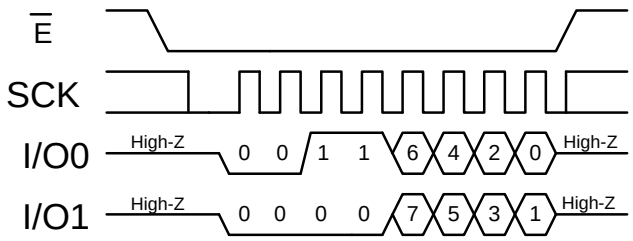
Bit	non-volatile	Definition
Bit 0 ($\overline{RDY}$)	no	The Ready bit indicates whether the memory is busy with a STORE or RECALL cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress. It is a read only bit
Bit 1 (WEN)	no	The Write Enable Latch bit indicates the status of the internal Write Enable Latch. When set to 1 with a Write Enable (WREN) instruction the internal Write Enable Latch is set, when set to 0 with a Write Disable (WRDI) instruction the internal Write Enable Latch is reset and no WRITE, Secure WRITE, WRITE Serial Number or WRITE Status Register instruction are accepted.
Bit 2 (BP0)	yes	The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against WRITE instructions. These bits are written with the WRITE Status Register (WRSR) instruction. When one or two or three of the Block Protect (BP2, BP1, BP0) bits are set to 1, the relevant memory area (see WRITE Status Register WRSR) becomes protected against all WRITE (WRITE, DIW, DIOW, QIW,QIOW, S_WRITE) instructions to the Memory Array. The Block Protect (BP2, BP1, BP0), Write Protect Enable (WPEN) and User Serial Number (PRSNR) bits can be written provided that the Hardware Protected Mode has not been set.
Bit 3 (BP1)	yes	
Bit 4 (BP3)	yes	
Bit 5 (SBP)	yes	Start block definition for protection, SBP=0 block protection will start with highest address, SBP=1 it will start with lowest address
Bit 6 (PRSNR)	yes	Protect User Serial Number
Bit 7 (WPEN)	yes	The Write Protect Enable bit is operated in conjunction with the WRITE Protect ($\overline{WP}$) signal. The Status Register WRITE Protect Enable (WPEN) bit and WRITE Protect ($\overline{WP}$) signal allow the device to be put in the Hardware Protected Mode (when the Status Register WRITE Protect Enable (WPEN) bit is set to 1, and WRITE Protect ($\overline{WP}$) is driven Low). In this mode, the non-volatile bits of the Status Register become read-only bits and the WRITE Status Register (WRSR) instruction is no longer accepted for execution.

READ Status Register (RDSR):

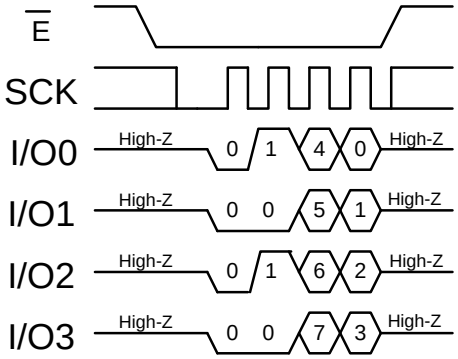
The READ Status Register instruction provides access to the status register. The READY/BUSY and WRITE Enable status of the device can be determined by the RDSR instruction. Similarly, the Block WRITE Protection bits, PRSNR and WPEN indicate the extent of protection employed. With SBP the start point for Block Protection can be set. These bits, besides $\overline{RDY}$ and WEN, are set by using the WRSR instruction. Status Register can be read out in SPI, DPI and QPI Mode with up to 108 MHz.



RDSR SPI Mode



RDSR DPI Mode



RDSR QPI Mode

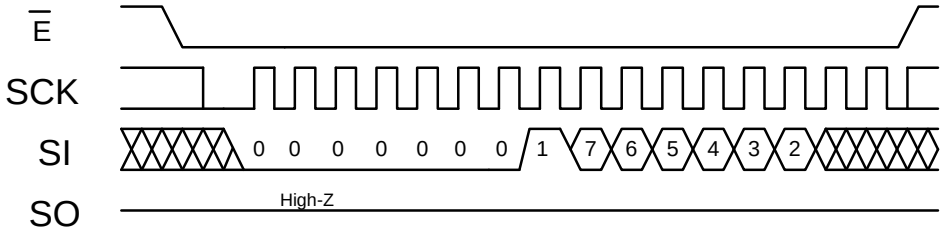
WRITE Status Register (WRSR):

The WRSR instruction allows the user to select different levels of Hardware or Software protection for the memory array or User Serial Number.

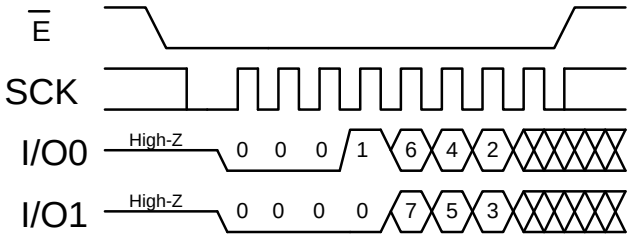
WREN command has to be sent prior to WRSR. The properties for access the Status Register are the same as the memory array. The WRSR instruction is volatile.

To make bit2 to bit7 non-volatile a STORE instruction has to follow the WRSR instruction. This STORE instruction is also valid for the memory array and all other non-volatile registers. Bit0 and bit1 are read-only.

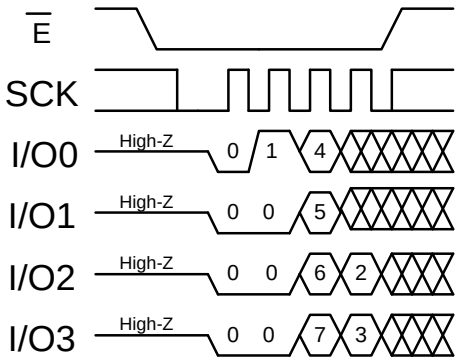
WRSR instruction can be executed in SPI, DPI and QPI Mode.



WRSR in SPI Mode



WRSR in DPI Mode



WRSR in QPI Mode

Block Protection

The device is divided into several array segments. Which and how many memory segments can be protected depends on the Status Register bits BP0,BP1 and BP2 together with the SBP bit. Any data within any selected segment will therefore be READ only. The block write protection levels and corresponding status register control bits are shown in the following table.

Level (Protected Block)	Status Register Bits			SBP Bit	Array Addresses Protected
	BP2	BP1	BP0		ANV32AA3P
0	0	0	0	0 or 1	None
upper 1/64	0	0	1	0	0x1F800 - 0x1FFFF
upper 1/32	0	1	0	0	0x1F000 - 0x1FFFF
upper 1/16	0	1	1	0	0x1E000 - 0x1FFFF
upper 1/8	1	0	0	0	0x1C000 - 0x1FFFF
upper 1/4	1	0	1	0	0x18000 - 0x1FFFF
upper 1/2	1	1	0	0	0x10000 - 0x1FFFF
lower 1/64	0	0	1	1	0x00000 - 0x007FF
lower 1/32	0	1	0	1	0x00000 - 0x00FFF
lower 1/16	0	1	1	1	0x00000 - 0x01FFF
lower 1/8	1	0	0	1	0x00000 - 0x03FFF
lower 1/4	1	0	1	1	0x00000 - 0x07FFF
lower 1/2	1	1	0	1	0x00000 - 0x0FFFF
whole array	1	1	1	0 or 1	0x00000 - 0x1FFFF

The WRSR instruction also allows the user to enable or disable the WRITE Protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware WRITE Protection Mode (HPM) is enabled when the $\overline{WP}$ pin is low and the WPEN bit is “1”. Hardware WRITE Protection Mode is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is “0”. When the device is hardware write protected, WRITE to the Status Register non-volatile bits (bit[2] to bit[7]) are disabled. This includes the Block Protect bits, SBP bit, the Serial Number Protection bit and the WPEN bit. The block-protected sections in the memory array are disabled. WRITE is only allowed to sections of the memory which are not block-protected.

When the WPEN bit is hardware write protected, it cannot be changed back to “0”, as long as the $\overline{WP}$ pin is held low.

The Write Status Register (WRSR) instruction has no effect on bit[1] (WEN) and bit[0] (RDY) of the Status Register.

Chip Enable ($\overline{E}$) must be driven High after the eighth bit of the data byte has been clocked in. If not, the Write Status Register (WRSR) instruction is not executed.

WPEN	$\overline{WP}$[b]	Mode	Protected Blocks [a]	Unprotected Blocks [a]	Status Register
0	H	Software Protected SPM	Protected	Writeable	Writable, if WEN=1, BP0, BP1, BP2, SBP, PRSNR and WPEN are writable
0	L		Protected	Writeable	
1	H		Protected	Writeable	
1	L	Hardware Protected HPM	Protected	Writeable	Protected, if WEN=1, no access to Status Register bit2 - bit7

[a] As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register.
[b] In QPI mode $\overline{WP}$ is forced LOW internally

Configuration Register

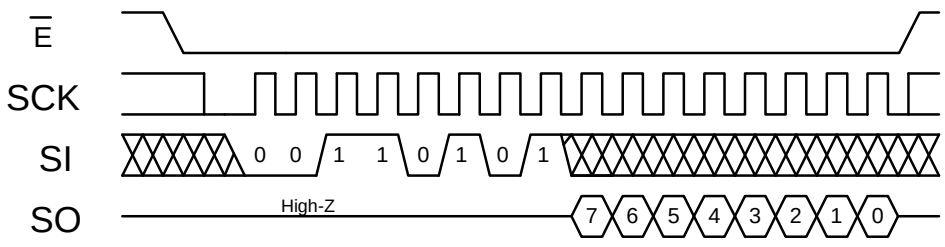
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PDIS		$\overline{\text{SWM}}$			SQM	

Configuration register is a 8 bit register with volatile and non-volatile bits. With $\overline{\text{SWM}}$ the success of a S_WRITE operation can be monitored, independent if WRITE has been executed in SPI, DPI or QPI mode. It is internally reset to 0 at the begin of each S_WRITE operation. PDIS=1 disables the PowerStore feature and during power down all volatile data, in the memory array as well as the in the non-volatile registers, get lost. With SQM the ANV32AA3P can be set in QPI Mode. After power-up the QPI mode is automatically set.

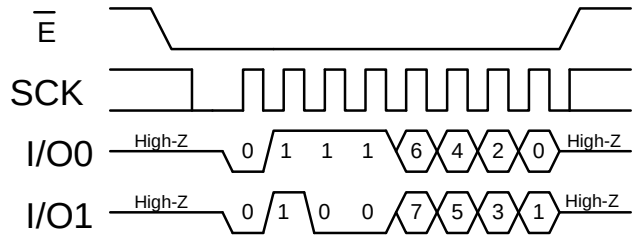
Bit	non-volatile	Definition
Bit 0	yes	must be set to 0
Bit 1 (SQM)	yes	SQM =1 Quad Mode; SQM = 0 no Quad Mode set non-volatile (SPI or DPI possible)
Bit 2		don't care
Bit 3		don't care
Bit 4 (SWM)	no	S_WRITE Monitoring bit indicates the success of the last Secure Write operation. With $\overline{\text{SWM}}$ = 0 Secure Write was successful, with $\overline{\text{SWM}}$ = 1 data and/or address were corrupt. Secure Write was ignored. It is a read only bit.
Bit 5		don't care
Bit 6 (PDIS)	yes	PDIS bit disables the PowerStore function
Bit 7		don't care

READ Configuration Register (RDCR)

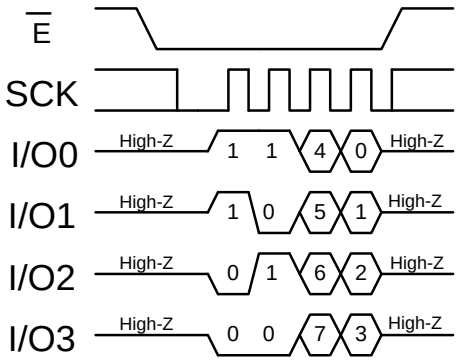
The READ Configuration Register instruction provides access to the Configuration Register. With CR[1] =1 the ANV32AA3P can be set non-volatile to QPI mode and will start after power-up in QPI mode. When CR[1]=0 the initial protocol will be SPI. SMW is a read-only bit which indicated the last Secure Write Operation. With PDIS CR[6]=1 the PowerStore function is disabled. Configuration Register can be read out in SPI, DPI and QPI Mode with up to 108 MHz.



RDCR in SPI Mode



RDCR in DPI Mode



RDCR in QPI Mode

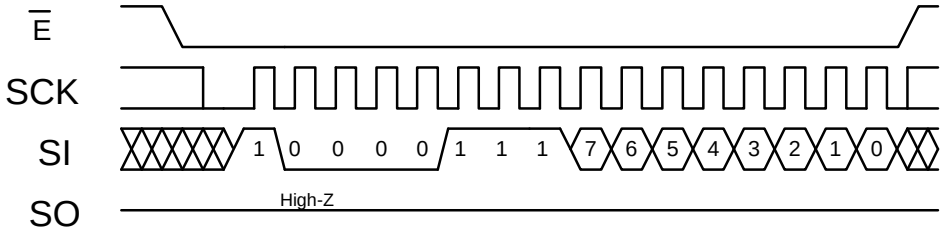
WRITE Configuration Register (WRCR)

The WRCR instruction enables access to the 2 non-volatile bits CR[1] and CR[6].

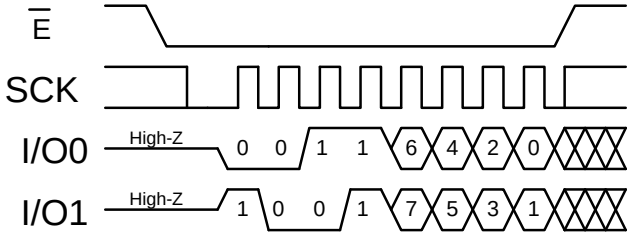
WREN command has to be sent prior to WRCR. The properties for access the Configuration Register are the same as the memory array. The WRCR instruction is volatile.

To make Bit1 and Bit6 non-volatile a STORE instruction has to follow the WRCR instruction. This STORE instruction is also valid for the memory array and all other non-volatile registers. SR[4] bit is read only.

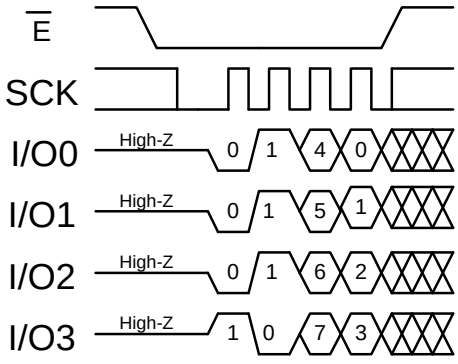
WRSR instruction can be executed in SPI, DPI and QPI Mode.



WRCR in SPI Mode



WRCR in DPI Mode



WRCR in QPI MODE

Read from Memory Array (READ):

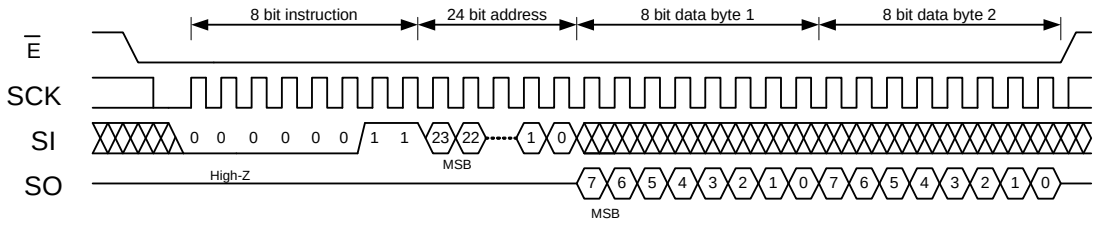
There are different READ Operations from memory array available, READ, F_READ, S_READ and FS_READ each in SPI, DPI and QPI mode. READ, F_READ are also available in SPI mode DOR, DIOR, QOR, QIOR.

READ

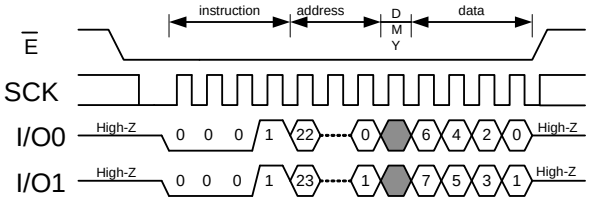
Reading the device requires the following sequence. After the $\overline{E}$ is pulled low to select a device, the READ operation code is transmitted followed by the 3 byte address to be read (A23 - A0). Address bits A23 - A17 are don't care. A16 is in the MSB bit[0]. A15 to A0 are in the following 2 address bytes.

Upon completion, any data on input data will be ignored on SI for SPI mode. In DPI mode I/O0 and I/O1 becomes outputs, in QPI mode I/O0, I/O1, I/O2 and I/O3 becomes also outputs. The data (D7 - D0) at the specified address is then shifted out onto SO (SPI), I/O0, I/O1(DPI) and I/O0, I/O1, I/O2, and I/O3 (QPI) with the falling edge of SCK. If only one byte is to be read, $\overline{E}$ should be driven high after the data comes out. The device is for READ operation always in block roll over mode, so that the READ sequence can be continued as long as $\overline{E}$ stays low, the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle. The READ operation can be executed up to 66MHz. In DPI and QPI mode a dummy Clock cycle has to be implemented after last address bit has been clocked in.

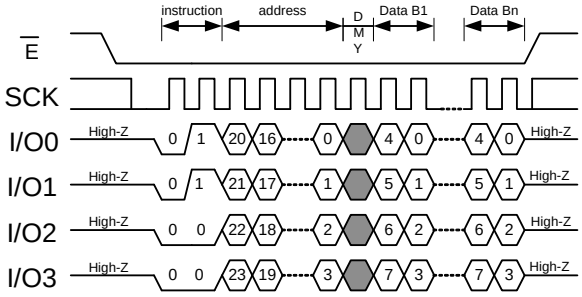
The READ cycle can be started when a WRITE, RECALL or STORE cycle is not in progress and terminated at any time driving the Chip Enable ($\overline{E}$) to High.



READ in SPI Mode 2 bytes



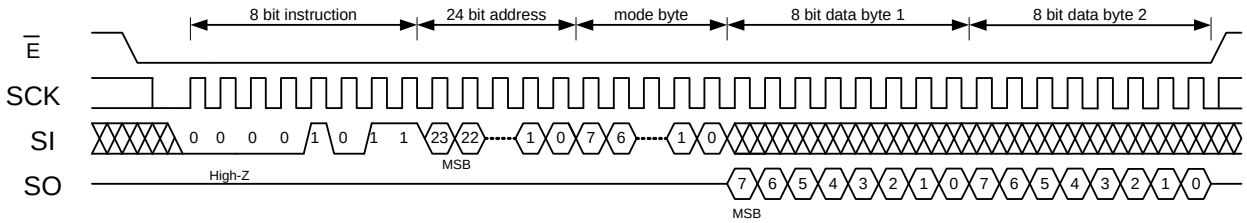
READ in DPI Mode single byte



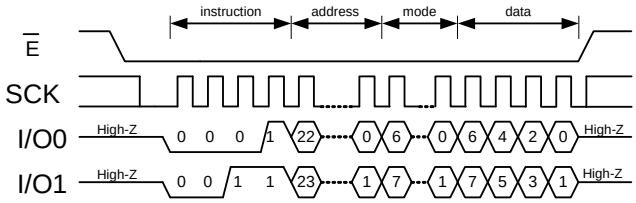
READ in QPI Mode multi byte access

Fast READ

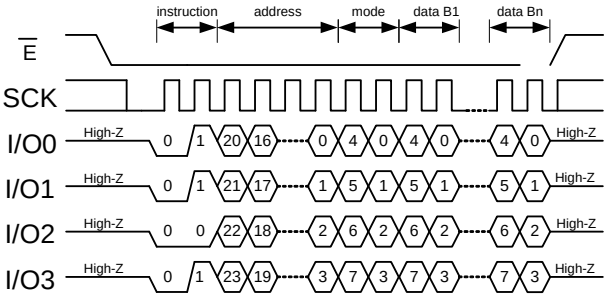
With F_READ the memory read out can be done up to 108MHz. Therefore the following sequence is required; After the $\overline{E}$ is pulled low to select a device, the F_READ operation code is transmitted followed by the 3 byte address (A23 - A0). Address bits A23 - A17 are don't care. A16 is in the MSB bit[0]. A15 to A0 are in the following 2 address bytes. Upon completion any input data will be ignored. Thereafter a mode byte will be clocked in independent from SPI, DPI or QPI mode. In DPI mode I/O0 and I/O1 become outputs, in QPI mode I/O0, I/O1, I/O2 and I/O3 become also outputs. The data (D7 - D0) at the specified address is then shifted out onto SO (SPI), I/O0, I/O1(DPI) and I/O0, I/O1, I/O2, and I/O3 (QPI) with the falling edge of SCK. If only one byte is to be read, $\overline{E}$ should be driven high after the data comes out. The device is for READ operation always in block roll over mode, so that the READ sequence can be continued as long as $\overline{E}$ stays low, the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle.



F_READ in SPI Mode



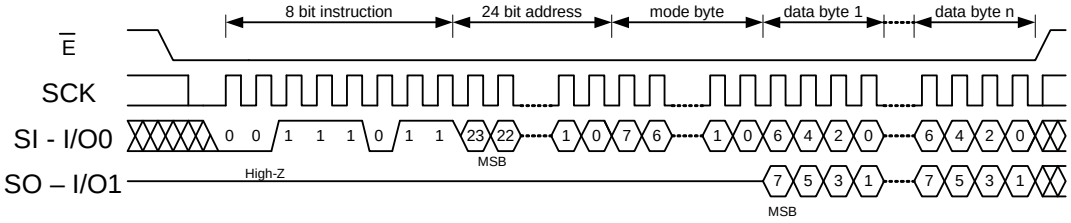
F_READ in DPI Mode



F_READ in QPI Mode

Dual Output READ

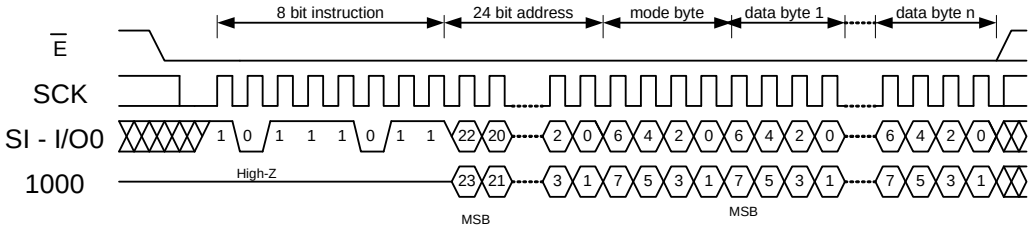
To increase the data rate in SPI mode the Dual Output READ instruction can be applied. After the $\overline{E}$ is pulled low to select a device, the DOR operation code is transmitted followed by the 3 byte address (A23 - A0). Upon completion any input data will be ignored. Thereafter a mode byte will be clocked in. SI becomes I/O0 and SO becomes I/O1. The data (D7 - D0) at the specified address is then shifted out onto I/O0 and I/O1 with the falling edge of SCK.



DOR instruction

Dual Input Output READ

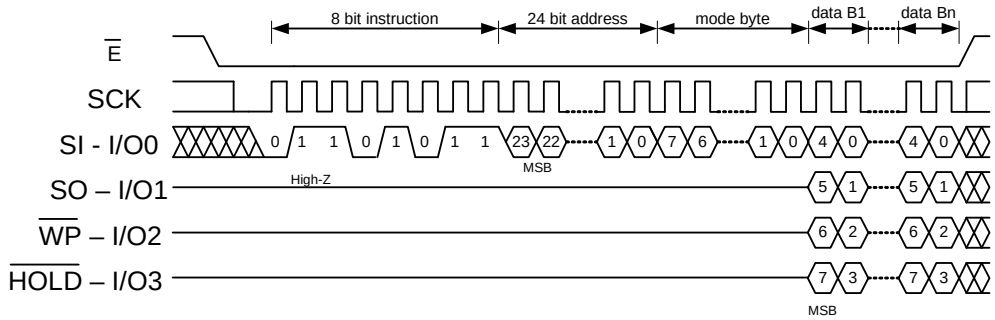
For DIOR instruction SPI mode has to be selected. After the $\overline{E}$ is pulled low to select a device, the DIOR operation code is transmitted in single mode followed by the 3 byte address (A23 - A0) in dual mode. SO becomes I/O1. Upon completion any input data will be ignored. Thereafter a mode byte also in dual mode will be clocked in. SI becomes I/O0. The data (D7 - D0) at the specified address is then shifted out onto I/O0 and I/O1 with the falling edge of SCK.



DIOR instruction

Quad Output READ

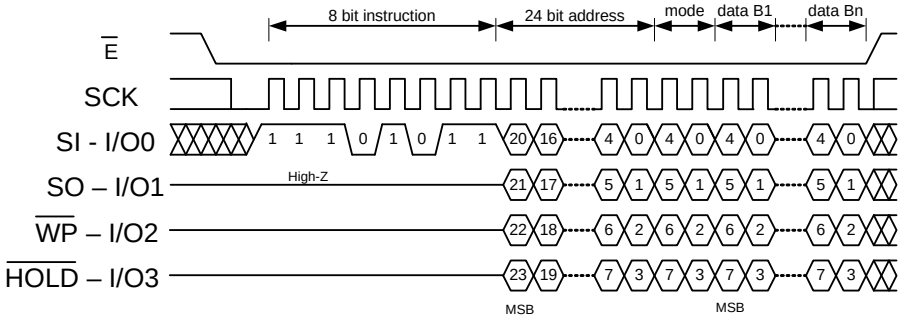
To further increase the data rate in SPI mode the Quad Output Read instruction can be applied. After the $\overline{E}$ is pulled low to select a device, the QOR operation code is transmitted followed by the 3 byte address (A23 - A0). Thereafter a mode byte will be clocked in. SI becomes I/O0, SO - I/O1, $\overline{WP}$ - I/O2 and $\overline{HOLD}$ - I/O3. Upon completion any input data will be ignored. The data (D7 - D0) at the specified address is then shifted out onto I/O0 to I/O3 with the falling edge of SCK.



QOR instruction

Quad Input Output READ

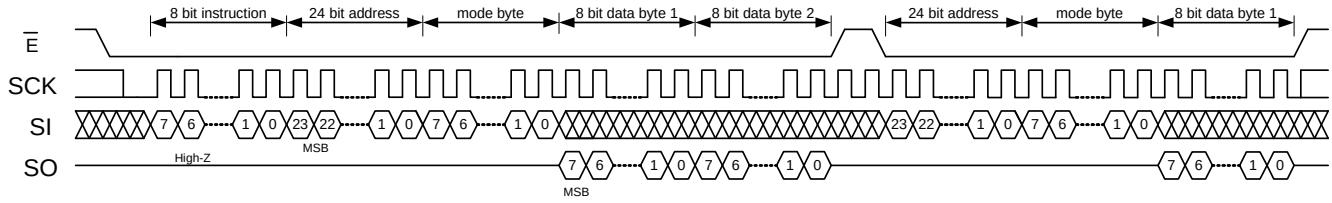
For QIOR instruction SPI mode has to be selected. After the $\overline{E}$ is pulled low to select a device, the QIOR operation code is transmitted in single mode followed by the 3 byte address (A23 - A0) in quad mode. SI becomes I/O0, SO - I/O1, $\overline{WP}$ - I/O2 and $\overline{HOLD}$ - I/O3. Thereafter a mode byte also in quad mode will be clocked in. Upon completion any input data will be ignored. The data (D7 - D0) at the specified address is then shifted out onto I/O0 to I/O3 with the falling edge of SCK.



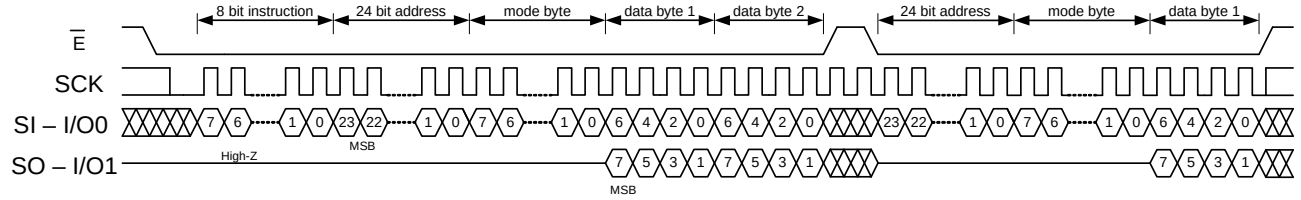
QIOR instruction

Execute In Place Operation (XIP)

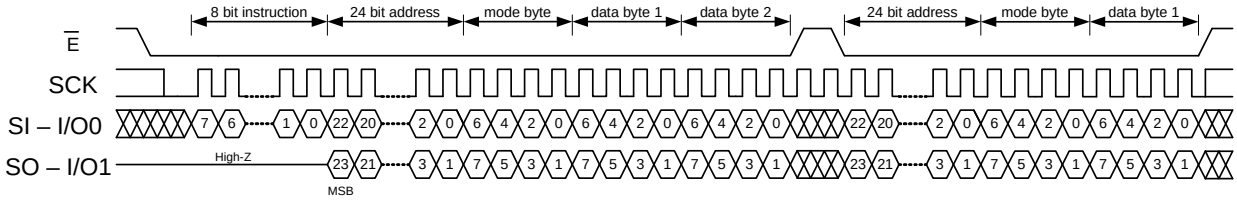
The mode byte for the following Fast READ operations in SPI, DPI and QPI mode can be used to step to different addresses in a random access without clocking in a read instruction again. XIP operations can also be done with DOR, DIOR, QOR and QIOR. First a 8 bit Fast Read instruction followed by the start read address has to be submitted. Mode Byte [0xAF] will activate XIP operation and data bytes can be clocked as described in the selected READ operation above. After the next falling edge of $\overline{E}$ the ANV32AA3P will remain in XIP operation mode and with submitting a new 24 bit address and a mode byte the addressed data can be read out. For mode byte [0xAF] this procedure can be repeated also after the next $\overline{E}$ controlled address change. In case mode byte [0xFF] has been transmitted the XIP operation will be reset with the next rising edge of $\overline{E}$ and after the next falling edge of $\overline{E}$ a new 8 bit instruction has to be submitted.



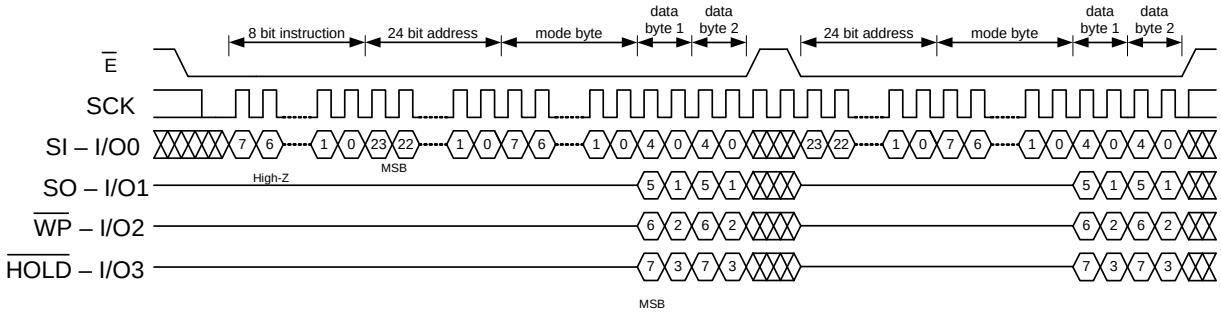
F_READ in SPI Mode (XIP)



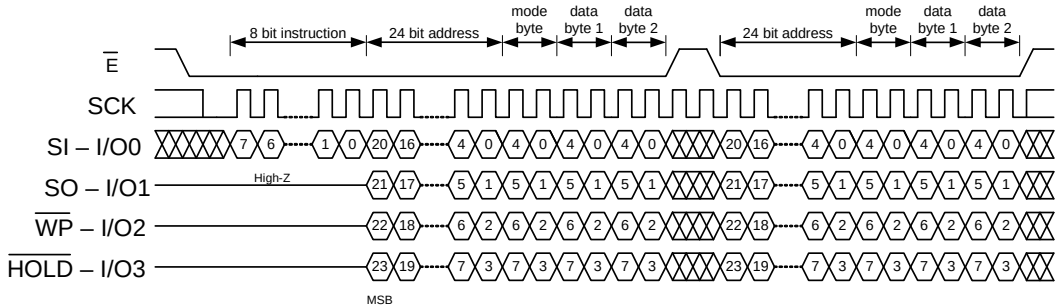
DOR in SPI Mode (XIP)



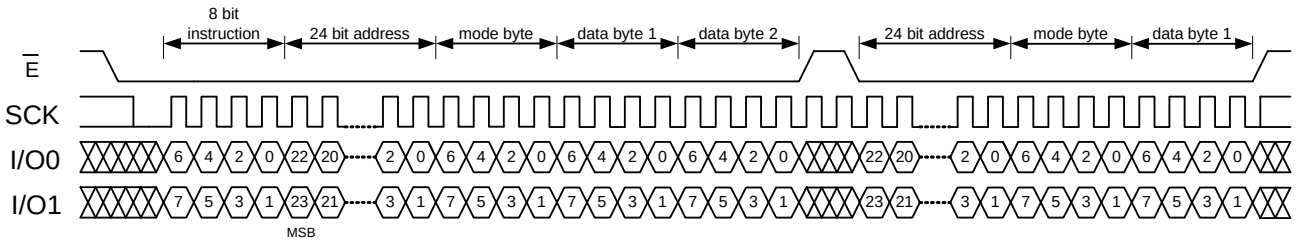
DIOR in SPI Mode (XIP)



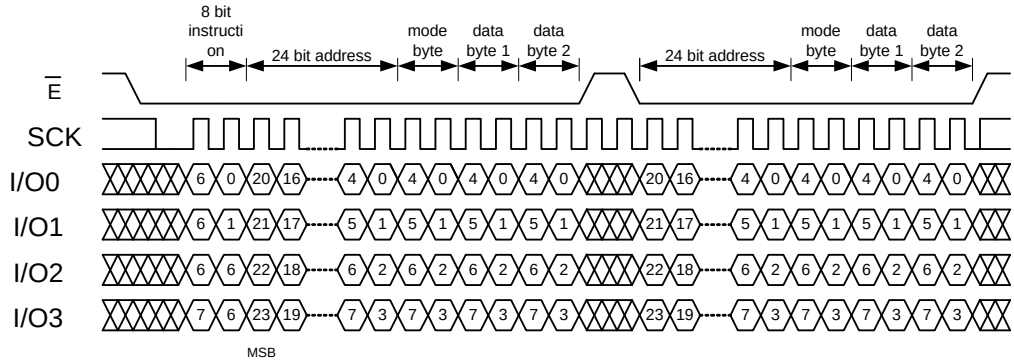
QOR in SPI Mode (XIP)



QIOR in SPI Mode (XIP)



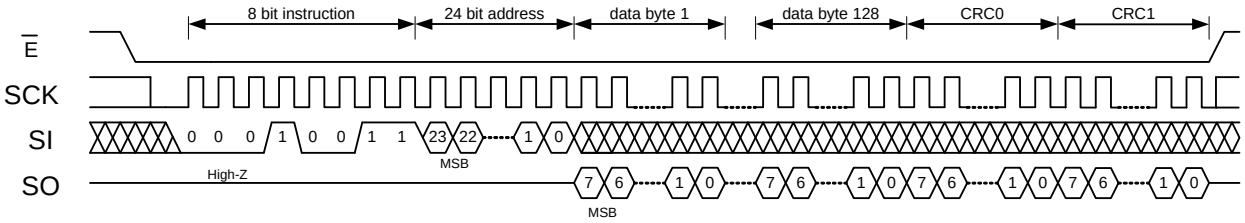
F_READ in DPI Mode (XIP)



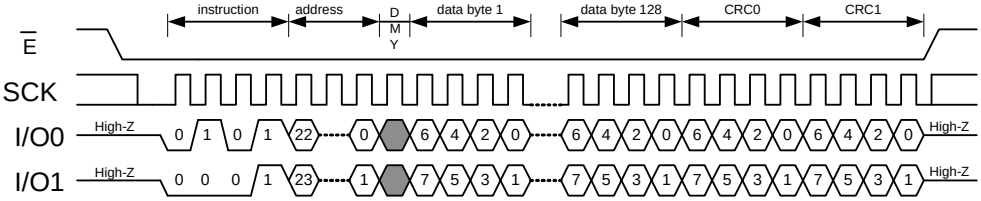
F_READ in QPI Mode (XIP)

Secure Read (S_READ):

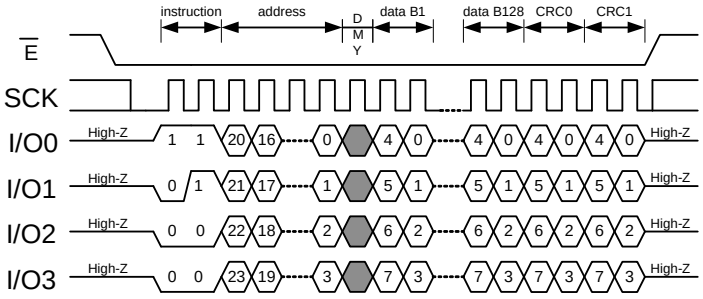
The secure READ operation is a 128 Byte data read out of the memory array. In parallel with the data transfer to the external bus internally a CRC is calculated, including the 3 Byte address and all 128 Byte data. After last byte is read the 16 bit CRC will be clocked out. All address bits are used for CRC calculation. The unused address bits have to be 0. The CRC16-CCITT polynomial $x^{16}+x^{12}+x^5+1$ is used for calculation. Page roll over is defined for Secure READ. The initial value is 0xFFFF. The checksum is transmitted with MSB first. Secure READ is available in SPI, DPI and QPI mode. S_READ is a 66MHz operation.



S_READ in SPI Mode



S_READ in DPI Mode

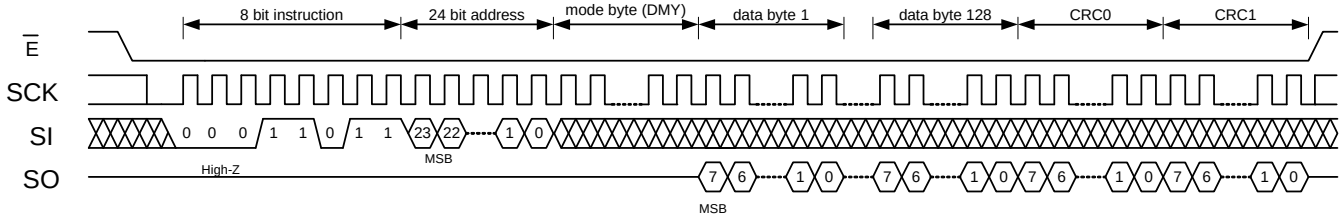


S_READ in QPI Mode

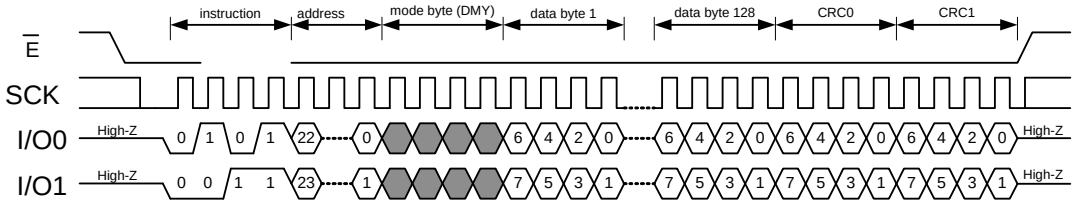
Fast Secure READ (FS_READ)

The Fast Secure READ operation is a 128 Byte data read out of the memory array. In parallel with the data transfer to the external bus internally a CRC is calculated, including the 3 Byte address and all 128 Byte data. After last byte is read the 16 bit CRC will be clokked out. All address bits are used for CRC calculation. The unused address bits have to be “0”. The CRC16-CCITT polynomial $x^{16}+x^{12}+x^5+1$ is used for calculation. Page roll over is defined for Fast Secure READ. The initial value is 0xFFFF. The checksum is transmitted with MSB first. Fast Secure READ is available in SPI, DPI and QPI mode. FS_READ is a up to 108MHz operation.

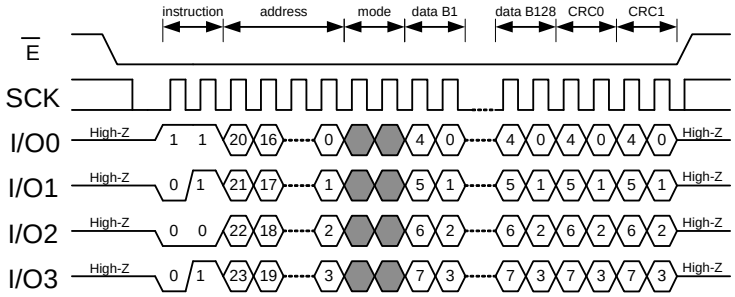
Therefore the following sequence is required; After the $\overline{E}$ is pulled low to select a device, the FS_READ operation code is transmitted followed by the 3 byte address (A23 - A0). Address bits A23 - A17 must be “0”. A16 is in the MSB bit[0]. A15 to A0 are in the following 2 address bytes. Thereafter a mode byte will be clocked in independent from SPI, DPI or QPI mode. In DPI mode I/O0 and I/O1 becomes outputs, in QPI mode I/O0, I/O1, I/O2 and I/O3 becomes also outputs. Upon completion any input data will be ignored. The data (D7 - D0) at the specified address is then shifted out onto SO (SPI), I/O0, I/O1(DPI) and I/O0, I/O1, I/O2, and I/O3 (QPI) with the falling edge of SCK. After completion read out of 128 Bytes the 2 CRC bytes will be clocked out.



FS_READ in SPI Mode



FS_READ in DPI Mode



FS_READ in QPI Mode

Write to Memory Array:

There are different WRITE operations to the memory array available, WRITE and S_WRITE, each in SPI, DPI and QPI mode as well as in SPI mode DIW, DI/OW, QIW, QI/OW.

In order to WRITE the device, two separate instructions must be executed. First, the device must be WRITE enabled via the Write Enable (WREN) Instruction. The status register bit[1] will be set to WEL=1. Then a WRITE Instruction may be executed. Also, the address of the memory location(s) to be written must be outside the protected address field location, selected by the Block Write Protection Level, otherwise these data will be ignored.

A WRITE Instruction requires the following sequence. After $\overline{E}$ is pulled low to select the device, a WRITE operation code is transmitted followed by the 3 byte address (A16 - A0, bit 23 to 17 are don't care) and the data (D7 - D0) to be written.

The part works in block roll over mode so that up to the whole memory array can be written with one command. After each byte of data is received, the address bits are internally incremented by one. All completely written bytes of an active page become valid when $\overline{E}$ pin is brought high or a new page starts or any STORE is initiated. Only the last incomplete written byte will be ignored.

Reaching the highest address the counter will roll over. This process can be continued until all data are written.

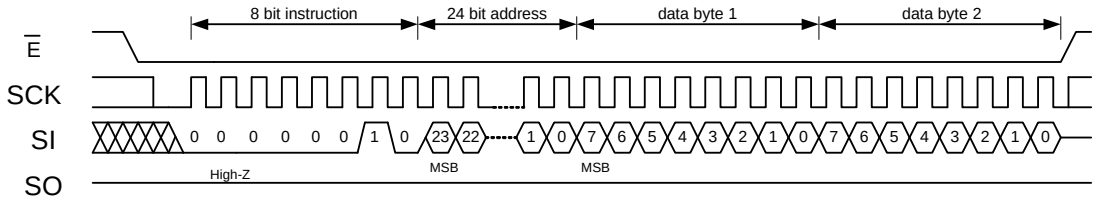
With the rising edge of $\overline{E}$ the device is automatically returned to the write disable state.

If the device is not Write enabled (WREN), the device will ignore any Write instruction and will return to the standby state, when $\overline{E}$ is brought high. A new $\overline{E}$ falling edge is required to reinitiate the serial communication.

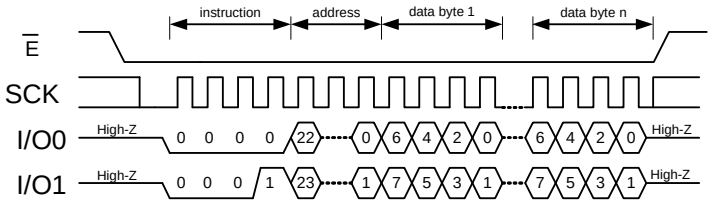
WRITE instructions can be executed up to 108 MHz. There are no dummy cycles required.

WRITE instruction

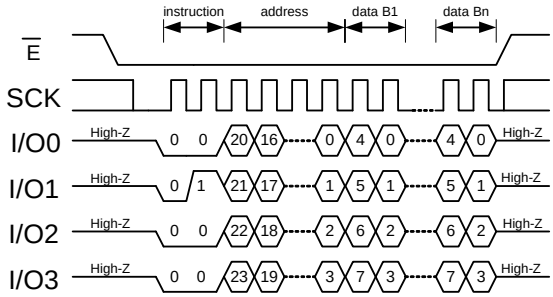
After WREN instruction has been executed $\overline{E}$ has to pulse low (select device) and the WRITE instruction will be clocked in (single, dual or quad mode) at SI, I/O0 - I/O1 or I/O0 - I/O3. Than the address and data will follow. Clocking in 3 address bytes requires 12 clock cycles in DPI mode and 6 clock cycles in QPI mode. Each data byte must be written with 8, 4 or 2 cycles respectively. The most significant bit will be clokked in during the first clock cycle on SI, I/O1 (DPI) or I/O3 (QPI).



WRITE in SPI Mode



WRITE in DPI Mode



WRITE in QPI Mode

Dual Input WRITE (DIW)

The DIW command is applicable in SPI mode and allows to clock in data on I/O0 and I/O1. Instruction and address will be transmitted via SI (I/O0) pin only in single mode. After last address has been clocked in, SI and SO becomes bidirectional I/O pins (I/O0 and I/O1).

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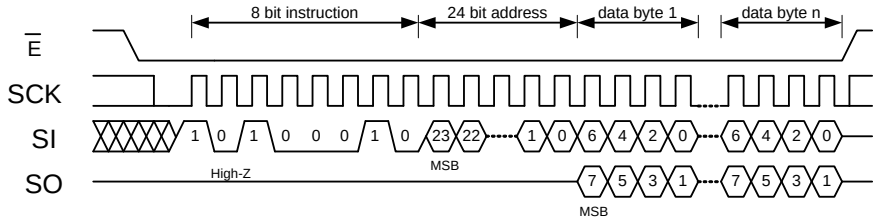
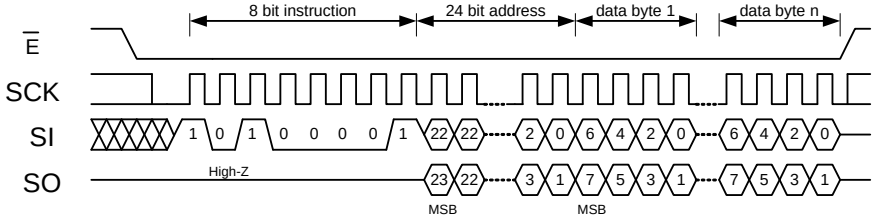


DIW instruction

DUAL Input Output WRITE (DIOW)

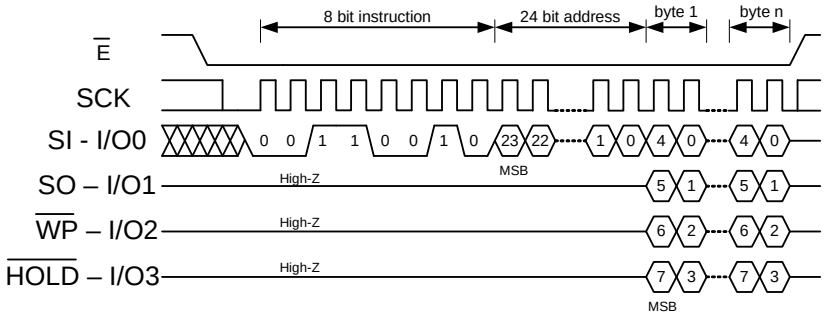
The DIOW command is applicable in SPI mode and allows to clock in address and data on I/O0 and I/O1. Instruction will be transmitted via SI (I/O0) pin only in single mode. After instruction has been clocked in, SI and SO becomes bidirectional I/O pins (I/O0 and I/O1).



DIOW instruction

QUAD Input WRITE (QIW)

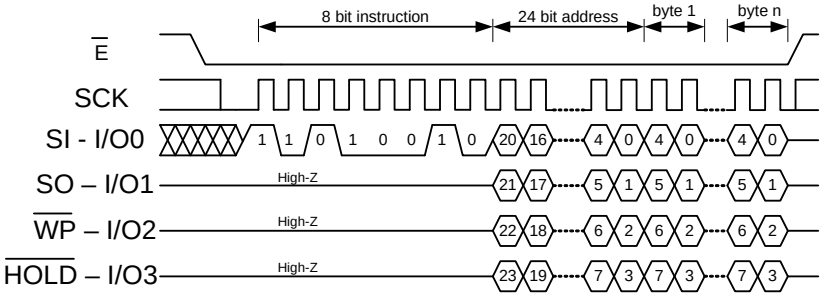
The QIW command is applicable in SPI mode and allows to clock in data on I/O0 to I/O3. Instruction and address will be transmitted via SI (I/O0) pin only in single mode. After last address has been clocked in, SI, SO, WP and HOLD becomes bidirectional I/O pins (I/O0 and I/O1).



QIW instruction

Quad Input Output WRITE (QIOW)

The QIOW command is applicable in SPI mode and allows to clock in address and data on I/O0 to I/O3. Instruction will be transmitted via SI (I/O0) pin only in single mode. After instruction has been clocked in, SI, SO, WP and HOLD becomes bidirectional I/O pins (I/O0 to I/O3)



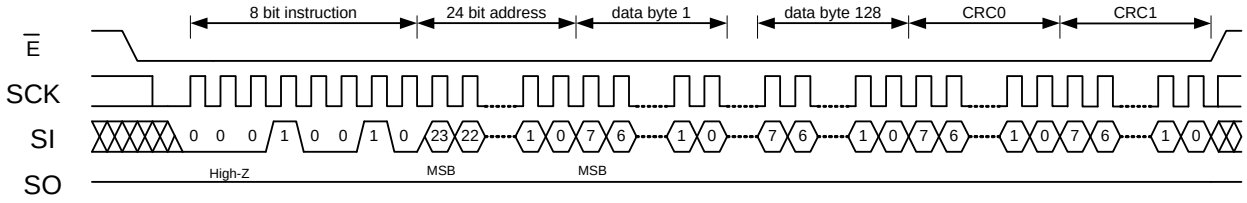
QIOW instruction

Secure WRITE Memory Array (S_WRITE):

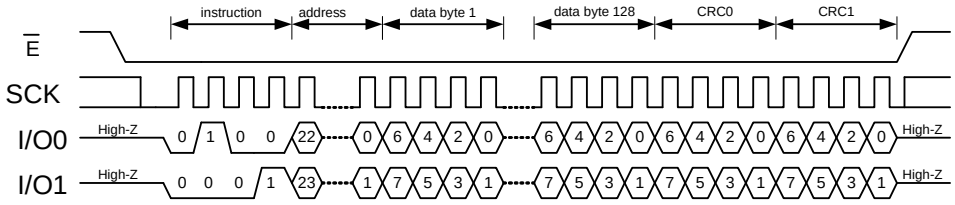
To enable the Secure WRITE operation a WREN has to occur first. Secure WRITE is a 128 Byte data WRITE to the memory array. A CRC is calculated, in parallel with the data transfer, from the 3 Byte address and 128 Byte data. Address bits 23 till 17 have to be 0. After last byte is written the 16 bit CRC has to be clocked in. All address bits will be used for CRC calculation. The CRC16-CCITT polynomial used is $x^{16}+x^{12}+x^{5}+1$. Page roll over is defined for Secure WRITE. The initial value is 0xFFFF. The checksum must be transmitted with MSB first. In addition the internally calculated CRC has to match the transmitted CRC. In this case data will be accepted. If the CRC's don't match data will be ignored, the existing memory data will stay and Configuration Register bit 4 will be set to 1. With RDSR the success of Secure WRITE has to be checked after every Secure Write operation and bit 4 is reset to 0 at the begin of next Secure Write operation.

With the Low-to-High transition of the $\overline{E}$ pin the device is automatically returned to the WRITE disable state.

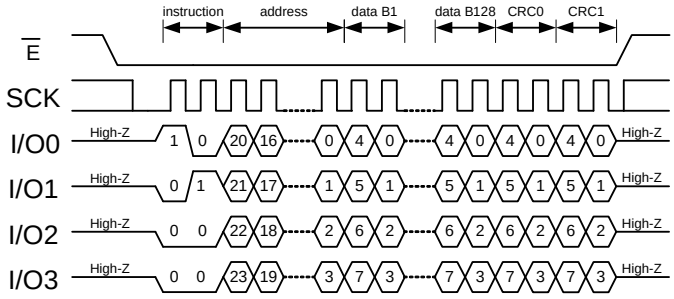
S_WRITE is available in SPI, DPI and QPI mode with operating speed up to 108MHz.



S_WRITE in SPI Mode



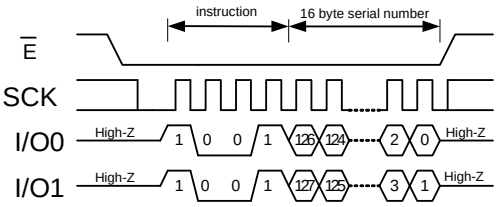
S_WRITE in DPI Mode



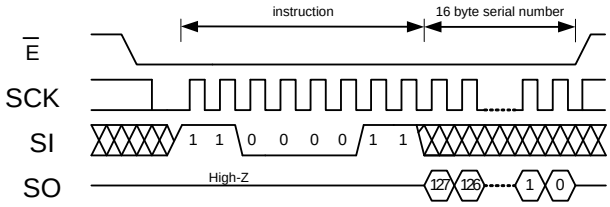
S_WRITE in QPI Mode

Read User Serial Number (RDSNR)

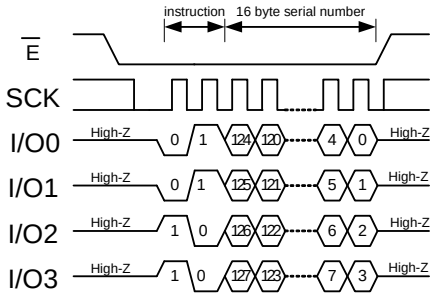
ANV32AA3P supports an additional non-volatile 16 byte register for a user-controlled serial number. With RDSNR register content can be read out up to 108MHz in SPI, DPI and QPI mode.



RDSNR in SPI Mode



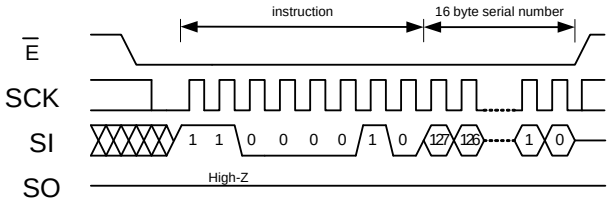
RDSNR in DPI Mode



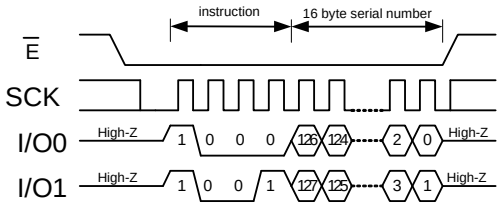
RDSNR in QPI Mode

WRITE User Serial Number (WRSNR)

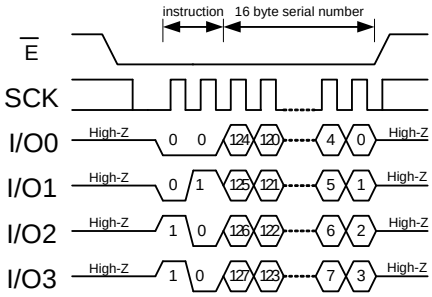
To enable the WRSNR operation a WREN has to occur first. With WRSNR a 16 byte user-controlled serial number can be written volatile to the register. All 128bit have to be clocked in completely otherwise the data will be ignored. With a STORE operation data in the register becomes non-volatile. The WRSNR command is available in SPI, DPI and QPI mode.



WRSNR in SPI Mode



WRSNR in DPI Mode



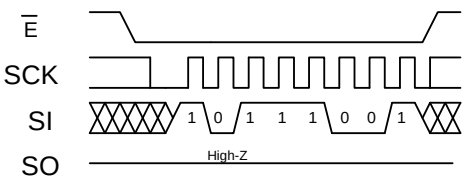
WRSNR in QPI Mode

Hibernate Mode:

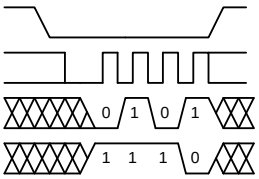
To enable the Hibernate Mode the Hibernate command has to be transferred. After $\overline{E}$ goes high the ANV32AA3P executes a STORE operation and will ignore any input signals until $\overline{E}$ goes low again. During HIBERNATE mode the part will consume only the current I_{SBH}.

With the falling edge of $\overline{E}$ an internal Power-Up RECALL cycle will be initiated and after this cycle is completed the device is ready for any operation.

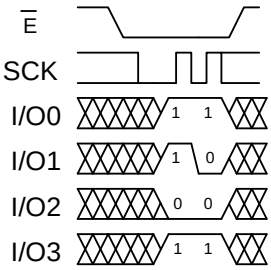
The enter Hibernate command can be executed in SPI, DPI and QPI mode.



Enter Hibernate in SPI Mode



Enter Hibernate in DPI Mode



Enter Hibernate in QPI Mode

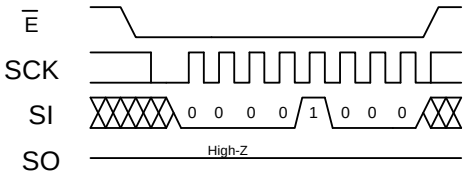
STORE

Data can be transferred from the SRAM to the non-volatile memory by a STORE command. During the STORE cycle, previous non-volatile data will be erased and then the new data stored into the non-volatile elements. Once a STORE cycle is initiated, further memory inputs and outputs are disabled until the cycle is completed. During a STORE operation, all commands will be ignored except the RDSR instruction.

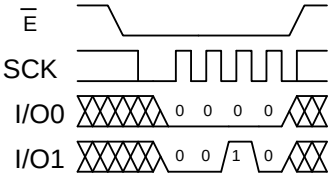
The READY/BUSY status of the device can be determined by initiating a Read Status Register (RDSR) instruction.

After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for any READ or WRITE operations.

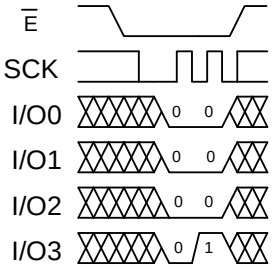
Instruction initiated STORE cycles are performed regardless of whether a WRITE operation has taken place after the last STORE or power-up and STORE is valid also for all non-volatile registers. STORE instruction can be submitted in SPI, DPI or QPI mode.



STORE instruction in SPI Mode



STORE instruction in DPI Mode



STORE instruction in QPI Mode

RECALL

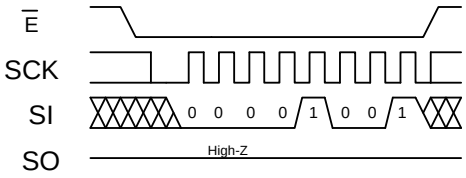
Data can be transferred from the non-volatile memory to the SRAM by a RECALL command.

Internally, RECALL is a two-step procedure. First, the SRAM data are cleared, and second, the non-volatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM will be activated for any operations. The RECALL operation in no way alters the data in the non-volatile storage elements.

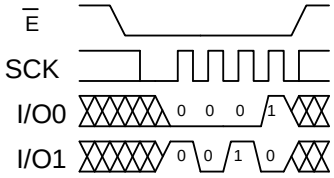
During an Recall operation, all commands will be ignored except the RDSR instruction.

The READY/BUSY status of the device can be determined by initiating a Read Status Register (RDSR) Instruction.

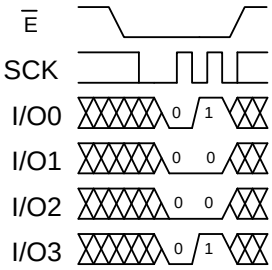
RECALL can be initiated in SPI, DPI and QPI mode.



RECALL in SPI Mode



RECAL in DPI Mode



Recall in QPI Mode

Hardware Store (HSB)

The hardware controlled STORE Busy pin ($\overline{HSB}$) is connected to an open drain circuit acting as both input and output to perform two different functions. When driven LOW by the internal chip circuitry it indicates that a STORE operation (initiated via any option) is in progress within the chip. When driven LOW by external circuitry for longer than $t_{w(H)S}$, the chip will conditionally initiate a STORE operation after $t_{dis(H)S}$.

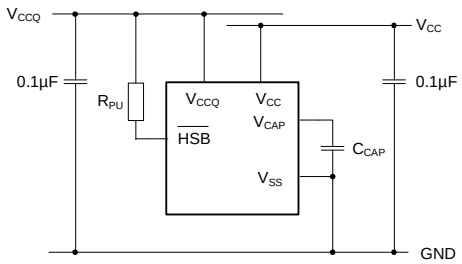
READ and WRITE operations that are in progress when $\overline{HSB}$ is driven LOW (either by internal or external circuitry) will be allowed to complete before the STORE operation is performed, in the following manner.

After $\overline{HSB}$ goes LOW, the part will continue normal SRAM operation for $t_{dis(H)S}$. During $t_{dis(H)S}$, a transition on any address or control signal will terminate SRAM operation and cause the STORE to commence.

Note that if an SRAM WRITE is attempted after $\overline{HSB}$ has been forced LOW, the WRITE will not occur and the STORE operation will begin immediately.

HARDWARE-STORE-BUSY ($\overline{HSB}$) is a high speed, low drive capability bidirectional control line.

In order to allow a bank of ANV32AA3P's to perform synchronized STORE functions, the $\overline{HSB}$ pin from a number of chips may be connected together. Each chip contains a small internal current source to pull $\overline{HSB}$ HIGH when it is not being driven LOW. To decrease the sensitivity of this signal to noise generated on the PC board, it may optionally be pulled to power supply via an external resistor with a value such that the combined load of the resistor and all parallel chip connections does not exceed $I_{\overline{HSB}OL}$ at V_{OL}.



Only if $\overline{HSB}$ is to be connected to external circuits, an external pull-up resistor should be used.

During any STORE operation, regardless of how it was initiated, the ANV32AA3P will continue to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete.

Upon completion of a STORE operation, the part will be disabled until $\overline{HSB}$ actually goes HIGH.

PowerSTORE Operation:

PowerSTORE operation is a unique feature of the SONOS technology that is enabled by default on the ANV32AA3P.

During normal operation, the device will draw current from V_{CC} for circuit operation and to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation

in case of power down. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CC}. A STORE operation will be initiated with power provided by the V_{CAP} capacitor.

If a Secure WRITE operation is in progress when V_{CC} drops V_{SWITCH} the complete transferred data of this ongoing Secure WRITE operation becomes invalid.

In the case of WRITE operation is in progress all complete written bytes are valid. Only the last incomplete written byte will be ignored. Above is shown the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the DC CHARACTERISTICS table for the size of C_{CAP}.

Power-Up RECALL:

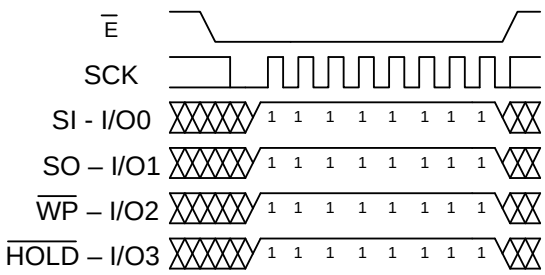
During power-up or after any low-power condition (V_{CC}<V_{SWITCH}), an internal RECALL request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and will take $t_{HRECALL}$ to complete. During Power-Up ReECALL operation, all commands will be ignored .

Default Recovery

The device can be reset from any mode to SPI by a default recovery sequence. Therefor all I/O pins, SI (I/O0), SO (I/O1), $\overline{WP}$ (I/O2) and $\overline{HOLD}$ (I/O3), have to be set to HIGH for 8 clock cycles.

To reduce un-needed non-volatile stores, Power STORE operation will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. The PowerSTORE Operation is valid for memory array and all non-volatile registers in parallel. The Read Status Register is disabled and no monitoring is possible when a Power STORE cycle is in progress.

The PowerSTORE function can also be disabled by setting PDIS of status register to 1.



Default Recovery Sequence

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to Ground . . . . . –0.5V to 2.4V
Voltage on V_{CC} Relative to Ground . . . . . –0.5V to 4.1V
Voltage on Input Relative to V_{CCQ} . . . . . –0.5V to (V_{CCQ} + 0.5V)
Temperature under Bias . . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C

Power Dissipation 0.5W
DC Output Current (1 output at a time, 1s duration) 15mA
Maximum accumulated storage time at 150°C . . . . . 0.3 years
Maximum accumulated time under Bias at 125°C . . . . . 0.5 years
Static discharge voltage (HBM) . . . . . > 2kV
Latch up current . . . . . > 100mA

a. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Symbol	Parameter	ANV32AA3P		Unit
		Min.	Max.	
V_{CC}	Core Supply Voltage	2.7	3.6	V
V_{CCQ}	I/O Power Supply Voltage	1.65	1.95	V

DC CHARACTERISTICS

V_{CC} / V = 2.7 - 3.6

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}	Average V_{CC} Current at 108 MHz		20		20	mA	Byte READ to Byte WRITE ratio 1:1 $V_{IN} \le 0.2V_{CCQ}$ or $\ge 0.8V_{CCQ}$ in QPI Mode
I_{CCQ1}[a]	Average V_{CCQ} Current at 108 MHz		1		1	mA	Byte READ to Byte WRITE ratio 1:1 $V_{IN} \le 0.2V_{CCQ}$ or $\ge 0.8V_{CCQ}$ in QPI Mode
I_{CC2}[b]	Average V_{CC} Current during *STORE*		2		2	mA	All Inputs Don’t Care, V_{CC} = max
I_{CC3}	Average V_{CC} Current at 66 MHz		5		5	mA	Byte READ to Byte WRITE ratio 1:1, $V_{IN} \le 0.2V_{CCQ}$ or $\ge 0.8V_{CCQ}$ in SPI Mode
I_{SB1}[c]	Average V_{CCQ} Current Standby		10		10	µA	$\overline{E} \ge V_{IH}$, Cycling input levels
I_{SB2}[c]	V_{CC} Standby Current		200		250	µA	$\overline{E} \ge (V_{CCQ} - 0.2V)$ All Others $V_{IN} \le 0.2V$ or $\ge (V_{CCQ} - 0.2V)$
I_{SBH}	Hibernate Standby Current		3		5	µA	on V_{CC} pin
I_{ILK}	Input Leakage Current		±3		±3	µA	V_{CCQ} = max $V_{IN} = V_{SS}$ to V_{CCQ}
I_{OLK}	Off-State Output Leakage Current		±3		±3	µA	V_{CCQ} = max $V_{IN} = V_{SS}$ to V_{CCQ}, $\overline{E} \ge V_{IH}$
V_{IH}	Input Logic “1” Voltage	$0.8V_{CCQ}$	V_{CCQ} + 0.5	$0.8V_{CCQ}$	V_{CCQ} + 0.5	V	All Inputs
V_{IL}	Input Logic “0” Voltage	V_{SS} – 0.5	$0.2V_{CCQ}$	V_{SS} – 0.5	$0.2V_{CCQ}$	V	All Inputs
V_{OH}	Output Logic “1” Voltage	V_{CCQ}-0.5		V_{CCQ}-0.5		V	I_{OUT} =– 2.0 mA
V_{OL}	Output Logic “0” Voltage		0.4		0.4	V	I_{OUT} = 2 mA
T_A	Operating Temperature	0	70	-40	85	°C	
C_{CAP}	Storage Capacitor	48	100	48	100	µF	6.3V (effective capacitance>27µF)
NV_C	non-volatile STORE operations	100		100		K	
$DATA_R$	Data Retention	100		100		Years	@55 °C

Note a: I_{CCQ_1} dependents on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note b: I_{CC_2} is the average current required for the duration of the respective *STORE* cycles (t_{STORE}).
Note c: $\overline{E} \ge V_{IH}$ will not produce standby current levels until any non-volatile cycle in progress has timed out.

Switching Characteristics	Symbol		Min.	Max.	Unit
	Alt.	IEC			
SCK Clock Frequency	f_{SCK}	f_C	0	108	MHz
Chip Enable Setup Time	t_{CSS}	$t_{su(E)}$	4		ns
/E High Time	t_{CS}	t_2	4		ns
/E Hold Time	t_{CSH}	$t_{h(E)}$	4		ns
Clock Setup time	t_{SKSH}	$t_{su(C)}$	2		ns
Clock High Time [d]	t_{CLH}	t_5	4		ns
Clock Low Time [d]	t_{CLL}	t_6	4		ns
Clock Rise Time	t_{RC}	t_7		60	ns
Clock Fall Time	t_{FC}	t_8		60	ns
Input Rise Time	t_{RD}			60	ns
Input Fall Time	t_{FD}			60	ns
Data Setup Time	t_{DSU}	$t_{su(D)}$	2		ns
Data Hold Time	t_{DH}	$t_{h(D)}$	2		ns
/HOLD Hold Time	t_{HH}	$t_{h(H)}$	2		ns
/HOLD Setup Time	t_{HSU}	$t_{su(H)}$	0		ns
Output Disable Time	t_{DIS}	$t_{dis(E)}$		8	ns
Clock Low to Output Valid	t_V	$t_{en(C)}$		6	ns
Output Hold Time	t_{HO}	$t_{h(D)}$	0		ns
/HOLD High to Output Low-Z	t_{LZ}	$t_{en(H)}$		6	ns
/HOLD Low to Output High-Z	t_{HZ}	$t_{dis(H)}$		6	ns

[e] $t_{CLH} + t_{CLL} \geq 1 / f_{SCK}$

AC TEST CONDITIONS

Input Pulse Levels	0V to 1.8V
Input Rise and Fall Times (10% - 90%)	≤ 1.8ns
Input and Output Timing Reference Levels	0.9V
Output Load	See Figure 1

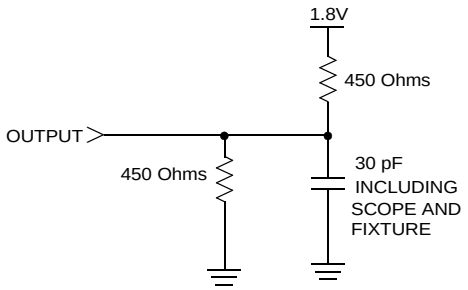


Figure 1. AC Output Loading

CAPACITANCE[d] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 1.8V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 1.8V

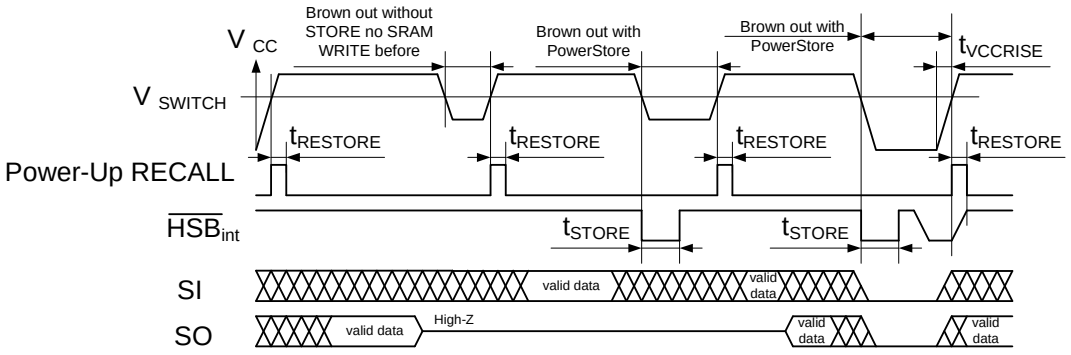
Note d: These parameters are guaranteed but not tested.

PowerStore/Power-Up RECALL

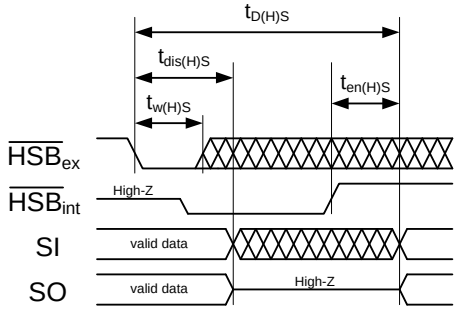
NO.	SYMBOLS		PARAMETER	ANV32AA3P		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
1	$t_{RESTORE}$		Power-up *RECALL* Duration		200	µs	e
2	t_{STORE}		*STORE* Cycle Duration		8	ms	
3	V_{SWITCH}		Low Voltage Trigger Level	2.3	2.65	V	
4	$t_{VCCRISE}$		V_{CC} rise time	100		µs	
5	t_{RECALL}		RECALL Duration (normal operating conditions)		50	µs	f
6	$t_{d(H)S}$	t_{HLQX}	*STORE* Cycle Duration HSB controlled		8	ms	
7	$t_{dis(H)S}$	t_{HLQZ}	$\overline{HSB}$ Low to Inhibit On	50		ns	
8	$t_{en(H)S}$	t_{HHQX}	$\overline{HSB}$ High to Inhibit Off		50	ns	
9	$t_{w(H)S}$	t_{HLHX}	External $\overline{HSB}$ Puls Width	20		ns	
10	I_{OUTH1}	$I_{HSB}OL$	$\overline{HSB}$ Output Low Current	3		mA	
11	I_{OUTH2}	$I_{HSB}OH$	$\overline{HSB}$ Output High Current	5	60	µA	

Note e: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
Note f: VCC > VCCmin

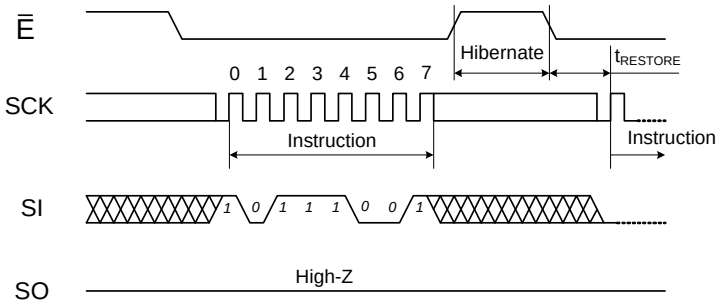
PowerStore/Power-Up RECALL



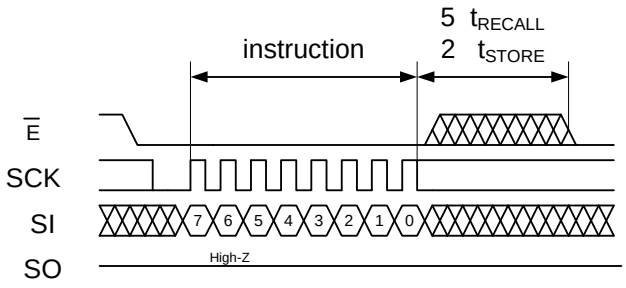
Hardware Controlled Store



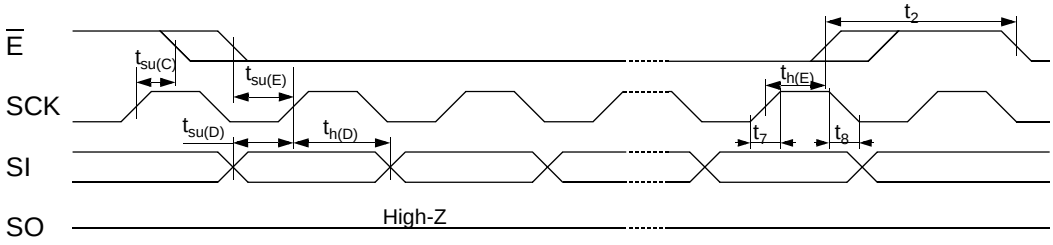
Hibernate



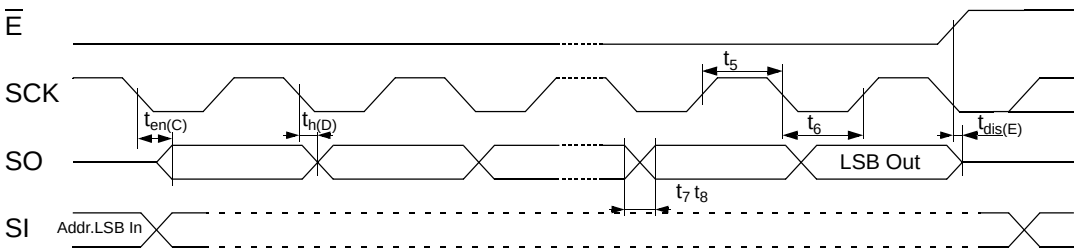
STORE/RECALL CYCLE ($V_{CC} > V_{CCmin}$)



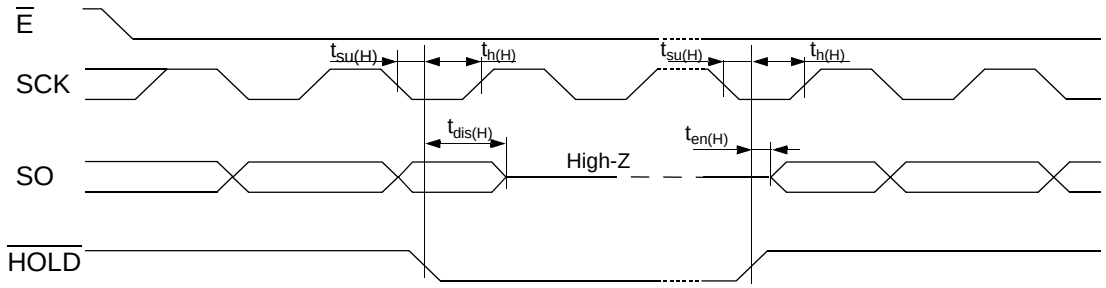
Serial Input Timing



Serial Output Timing



Hold Timing



Product Versions

The ANV32AA3P is available with the following feature sets:

- Supply voltage range 2.7V to 3.6V

Initial Delivery State

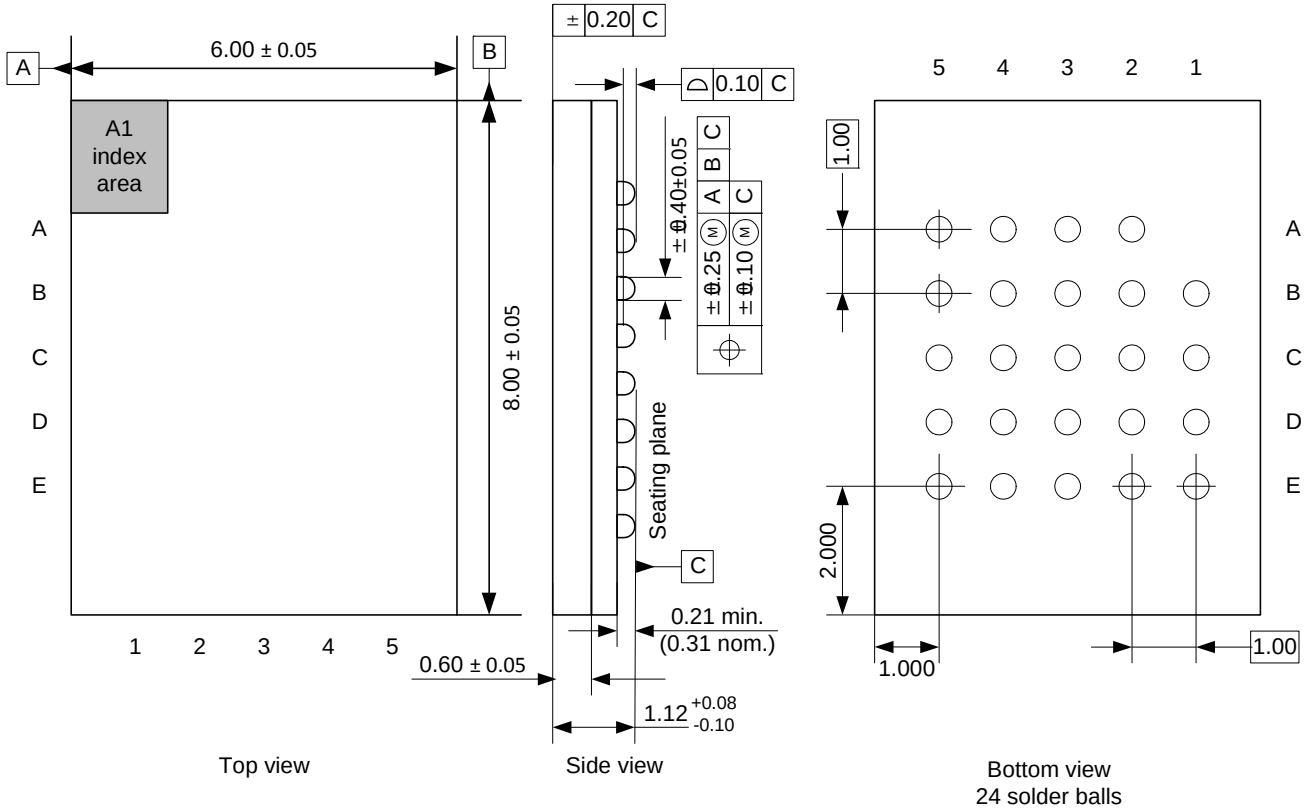
The device is delivered with Status Register 00xx00xx, non-volatile memory array „0“.

NOISE CONSIDERATIONS

The ANV32AA3P is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CCQ} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

Package

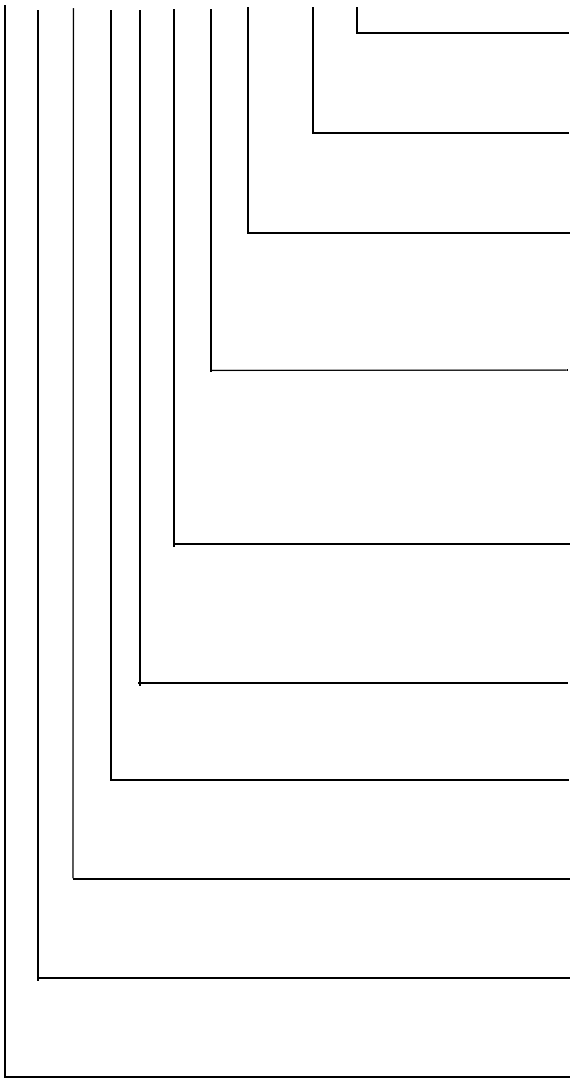
24 Ball FBGA (6x8)



Symbol	mm			inches		
	typ.	min.	max	typ.	min.	max.
A	0.85	0.8	0.9	0.0335	0.0315	0.0354
A1	0.02	0.00	0.05	0.0008	0.0000	0.0020
A2	0.20			0.0079		
A3		0,20			0.0079	
b	0.40	0.35	0.45	00157	0.0138	0.0177
D	5.00			0.1969		
D2	4.20	4.10	4.30	0.1654	0.1614	0.1693
E	6.00			0.2362		
E2	3.40	3.30	3.50	0.1339	0.1299	0.1378
e	1.27			0.0500		
L	0.45	0.50	0.55	0.0177	0.0197	0.0217

Ordering Information

ANV 3 2 A A 3 P B C 108 _



Lead Finish
Blank = SAC 105

Clock Rate
108= 108MHz

Temperature Range
C = Commercial (0 to 70°C)
K = Industrial (-40 to 85°C)

Package
B = BGA24

Power Supply
P= 2.7V ... 3.6V / 1.65V ... 1.95V

Interface
3 = QPI

Density
A = 1Mb

Version
A = initial version

Store Type
2 = PowerStore

Memory Type
3= serial nvSRAM

Document Revision History

Revision	Date	Summary
1.0	**June 2018**	initial version

Anvo-Systems Dresden ANV32AA3P Datasheet, June 2018

OCEAN CHIPS
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